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Research project to study cadmium selenide (CdSe) solar cells

Behrang Bagheri
Iowa State University

Research project to study cadmium selenide (CdSe) solar cells

by

Behrang Bagheri

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Program of Study Committee:
Vikram L. Dalal, Major Professor
Mani Mina
Rana Biswas
Jaeyoun Kim
Ruth Shinar

The student author, whose presentation of the scholarship herein was approved by the program of study committee, is solely responsible for the content of this dissertation. The Graduate College will ensure this dissertation is globally accessible and will not permit alterations after a degree is conferred.

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2020

DEDICATION

I would like to dedicate this dissertation to my wife Seyedeh Shaghayegh Jalalian, for all her love and support. I also would like to dedicate this work to my mother Hajieh Khanom Esmailzadeh and my father Abasal Bagheri for their love, endless support and encouragement. Finally, I would like to thank to my sisters Khatere Bagheri and Azadeh Bagheri, also my brother Mohamad Bagher Bagheri. This work is not possible without their support and sacrifice and I won't be the same person that I am today.

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TABLE OF CONTENTS

Page

LIST OF FIGURES

LIST OF TABLES

NOMENCLATURE

Isc	Short-circuit current
Jsc	Short-circuit current density
Voc	Open-circuit voltage
FF	Fill factor
PCE	Power-conversion efficiency
Rs	Series resistance
Rsh	Shunt resistance
ETL	Electron transport layer
HTL	Hole transport layer
ITO	Indium Tin Oxide
Cd	Cadmium
Se	Selenium
CdSe	Cadmium Selenide
CdS	Cadmium Sulfide
CdS:In	Indium doped Cadmium Sulfide
CdCl2	Cadmium Chloride
ZnTe	Zinc Telluride
NiO	Nickel Oxide
ZnO:Al	Aluminum doped Zinc Oxide
Si	Silicon
c-Si	Crystalline silicon
a-Si	Amorphous silicon

P3HT	Poly(3-hexylthiophene-2,5-diyl)
PTAA	Poly (triaryl amine), Poly[bis(4-phenyl) (2,4,6- trimethylphenyl) amine]
PCBM	Phenyl-C61-butyric acid methyl ester
SMU	Source Measure Unit
CV	Capacitance vs Voltage measurement
CF	Capacitance vs Frequency measurement
CFT	Capacitance-Voltage-Temperature measurement
QE	Quantum efficiency
EQE	Quantum efficiency

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ABSTRACT

Solar energy is the first useful, abundant, environmentally friendly and efficient source of renewable energy in the world. The conversion of solar energy into electricity using photovoltaic (PV) technology is clearly an important way, with significant potential to mitigate global warming by lowering the emission of greenhouse gases. The costs of the PV system are determined by the overall cost of the technology, such as structural costs, field wiring and the costs of chemical encapsulation materials. In order to remarkably reduce the total costs of solar PV technology, the conversion efficiency needs to be increased from the current ~15-20% to above 30%, because most of the systems costs reduce proportionately with the reduction in material consumption and the increase in conversion efficiency. The best way to achieve such higher efficiencies is to use a tandem junction solar cell, comprising two materials, one with a high bandgap as top cell and another with a lower bandgap as bottom cell. In this project, we will investigate the fundamental optical and electronic properties of an inorganic material, CdSe, then make proof-of-concept heterojunction solar cells in this material.

Among the properties to be studied will be doping concentration, mobility of electrons and holes, deep defect densities and recombination phenomena, minority carrier diffusion lengths, electron affinities and energies of band edges. Structural, electronic and optical measurement techniques will be used to measure the relevant properties. CdSe films will be deposited using multi-source evaporation techniques.

CdSe is an II-VI group semiconductor chalcogenide which can be considered as one of the most successful materials for photovoltaic and optoelectronic applications. CdSe is more appropriate for photovoltaic application compare to other inorganic compound semiconductor. Especially easy to deposit using mass-production vapor deposition techniques. It is binary

compound-by definition, stoichiometry easier to achieve than in ternary of quaternary. CdSe is not water soluble and does not thermally decompose, also it has reliable optical and electrical properties, like direct bandgap and high absorption coefficient in the visible range which makes it a good candidate as an absorber layer for solar cells.

In the first part of this work, we have shown the deposition of CdSe thin films using thermal evaporation method at high growth temperature of 400°C. The transmittance and reflection were analyzed with Cary 5000 UV-Vis-NIR spectrophotometer. The optical measurement shows CdSe is a direct band gap material with a perfect optical band gap of 1.72eV and high absorption coefficient about $\alpha \approx 9\times10^{4}cm^{-1}$ for higher energy photons range which is in the range needed to make tandem cells with crystalline silicon (c-Si).

In the next part, we study the critical processes like Cadmium Chloride ($CdCl_2$) treatment and Post-deposition selenization to improve the electrical properties of CdSe thin films. $CdCl_2$ activation process is a vital step which reduces the density of mid-gap states inside the bandgap and helps to obtain recrystallization, grain-growth and passivation of grain boundaries and also prevents from recombination. CdSe thin films were deposited on fluorine doped thin oxide (FTO) glass substrate at different thicknesses and their grain size and mobility were systematically analyzed before and after $CdCl_2$ activation using scan electron microscopy (SEM) and space charge limited current (SCLC) techniques respectively. $CdCl_2$ activated CdSe films showed larger grain size (from 0.9 to 1.9µm) and higher electron mobility (from 0.09 to $3.52cm^2/V.s$) by increasing film thicknesses (from 0.5 to 3µm) respectively. Post-deposition selenization of CdSe thin films shows much larger grain size (from 0.3 to 5.7µm), higher photoconductivity value (from 2.94×10^{-4} to 1.21×10^{-3} $\Omega^{-1}.cm^{-1}$) and higher mobility lifetime product for electron as majority

carrier (from 1.37×10^{-6} to 5.62×10^{-6} cm^2/V) by increasing the selenization time (from 0 to 120min) respectively.

In the last part of this thesis, we have studied, designed and fabricated the efficient heterojunction CdSe solar cell. We developed new NP superstrate and substrate device structure with different n-layer and p-layer such as n-CdS and p-PTAA, and p-PEDOT:PSS. In addition, cadmium chloride and post-deposition selenization were developed to passivate the recombination centers. 2µm grains were achieved under $CdCl_2$ treatment (at 500C for 10h). The highest Voc (world record) ever achieved in CdSe solar cells (0.8V) and current density $8mA/cm^2$. Moreover, we found dopant density, optical bandgap, urbach energy, shallow and deep traps equal to 2.5×10^{15} cm^{-3}, 1.7eV, 15.6meV, 0.24eV and 0.53eV respectively. Attempt-to-escape frequency and relative dilectric constant (ϵ_r) were measured 2×10^9Hz and 10.4 respectively.

CHAPTER 1. INTRODUCTION TO RENEWABLE ENERGY, SOLAR ENERGY AND SOLAR CELLS

1-1 Thesis Structure

In chapter one, introduction to energy, renewable energy, solar energy, photovoltaic and solar cell have been discussed. Also, it explains briefly on the planetary energy reserves, the world total energy consumption and photovoltaic share of global electricity production.

Second chapter, describes the general device physics and basic working principal of solar cells. Chapter three, dedicated to different characterization techniques of solar cells. Chapter four, CdSe thin film deposition and optical and electronic characterization. Chapter five, making proof of concept appropriate hetero-structure solar cell

1-2 Energy

Energy is the life power of the entire human civilization which is an essential factor for industrial revolution and technological development. The demand for energy is increasing along with high levels of world-wide population growth.

Total energy consumption is correlated with gross national product (GNP) and climate. The most highly developed countries, such as the United States, Germany and Japan have energy consumption rate of 7kW, 3.8kW and 3.6kW per person respectively. Consumption rate in developing countries, especially those in tropical area like India is about 0.7kW per capita. The US consumes 25% of world's energy with 5% of world population. On the other hand, China has the most significant growth of energy consumption at 5.5% per year which has 20% of world population (see Figure 1-1) [1].

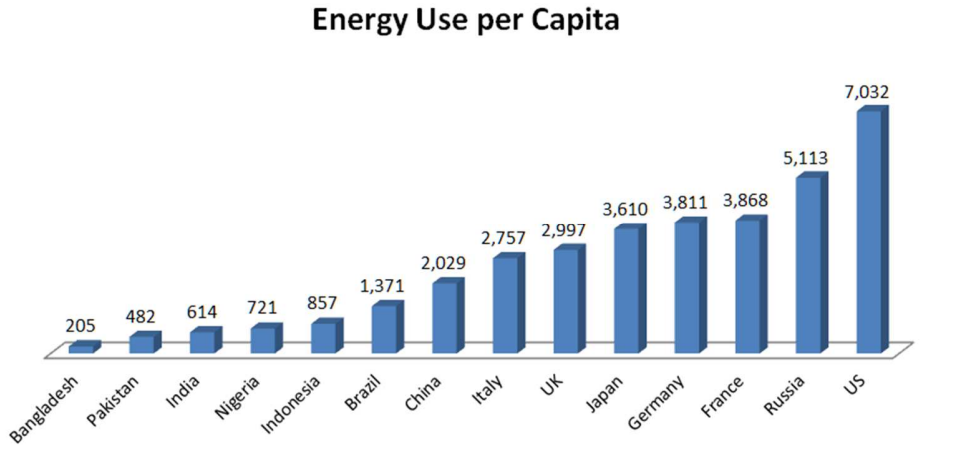

Figure 1-1 Energy use per capita, world population prospects [1].

1-3 Nonrenewable and Renewable Energy

There are two main areas of energy resources such as nonrenewable and renewable energy. Fossil fuels are the most nonrenewable energy sources which carbon is the main element in that. Fossil fuels like coal, oil, petroleum, natural gas and nuclear are available in limited supplies and take long time (hundreds millions of years) for them to be replenished. Formation process of fossil fuels is belong to long time ago even before the dinosaurs. Planets and plankton grew in ancient wetland (shallow seas and swampy forests). They created energy by absorbing sunlight. There was a huge source of energy in the bottom of the sea after those animals and plants died. Over the long period of time, dead plants and animals under high enough heat and pressure underground turned in to fossil fuels. Inexpensive extractions process, easy to store and ship anywhere in the world make fossil fuels a valuable source of energy. However, fossil fuels are not environmental friendly. Burning the fossil fuels pollute the land, water and air by releasing particles. Combustion of fossil fuels releases and increases carbon dioxide level inside atmosphere which is one of primary reason for greenhouse effect [2].

Renewable energy is energy from inexhaustible resources that replenished naturally over relatively short periods of time. The amount of renewable energy is limited per unit time. The five major renewable energy resources are biomass (includes: wood, municipal solid waste, landfill gas and biogas, ethanol and biodiesel), hydropower (water), geothermal, wind and solar [3].

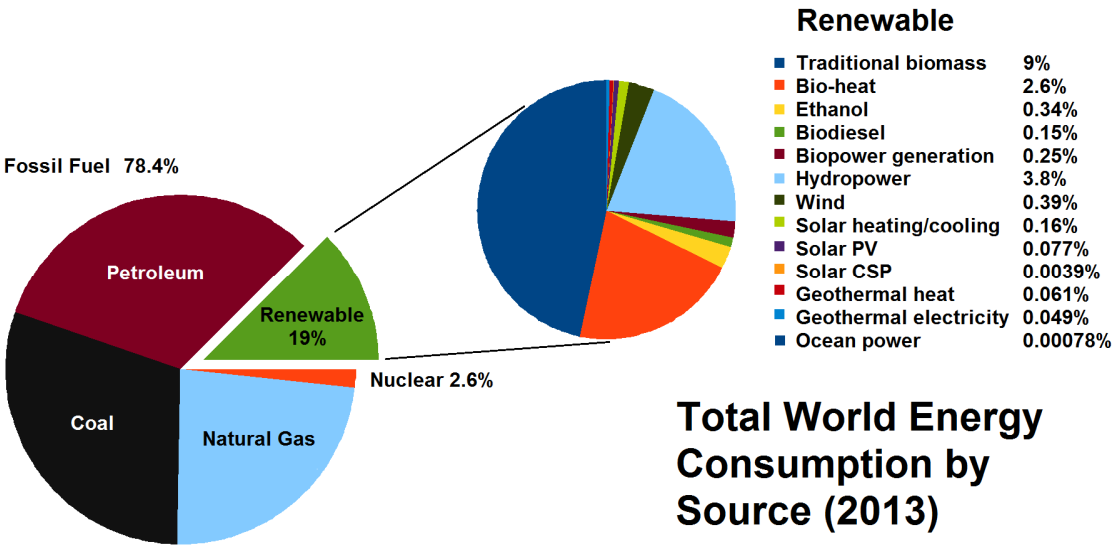

Figure 1-2 Total world energy consumption by source in 2013 [4].

According to renewables 2014 global status report, the world renewable energy consumption share was only 19% of the world total energy consumption. About 78.4% was coming from other three non-renewable resources including petroleum, coal, and natural gas. The rest of 2.6% was belong to nuclear source [4].

1-4 Solar Energy

Solar energy is an electromagnetic form of energy which is produced or radiated by the sun. Solar energy can be obtained by capturing light or heat from the sun. Solar energy is harnessed using a different range of advanced technologies like photovoltaics, solar heating, solar thermal energy and molten salt power. Solar energy is an outstanding source of renewable

energy. It is considered as a green technology because mainly it doesn't generate greenhouse gases.

Solar technology is broadly classified in two categories such as active or passive solar. Both systems perform the same function but under different performance and setups. Active solar techniques depend on external devices to harness the energy, including photovoltaic systems, concentrated solar power and solar water heating. Active solar systems have some drawbacks like, required expensive equipment, high maintenance cost and potential of releasing the toxins fluids (for storing heat) in the environment. Passive solar techniques don't rely on external devices. They are based on thermodynamics laws which transfer heat from warmer to cooler areas. Passive systems depend on the overall orienting of a building to the sun, thermal mass of materials, light-dispersing properties, and designing spaces that naturally circulate air. As a positive point, the entire setup of passive solar system is cheap but the efficiency directly depends on the weather condition [5]. Solar energy has many unique advantages:

- Solar energy is clean and environmental friendly that causes no greenhouse gasses.
- Solar energy is renewable that is abundant and available every day of the year.
- Solar energy is cheap, low solar panels maintenance cost over 30 years.
- Job creation, solar industry creates many jobs involved in site specific fabrication and installation.
- Local and national energy independence which allows individual to produce their own energy.
- Solar power is reliable because it works with a predictable energy source.
- Solar energy is low noise, sustainable and provides energy security.

Figure 1-3 compares the reserves of the finite energy resources with the yearly potential of the renewable alternatives. According to side by side view, each sphere and its volume are correspond to the total amount of energy recoverable from finite reserves and renewable sources.

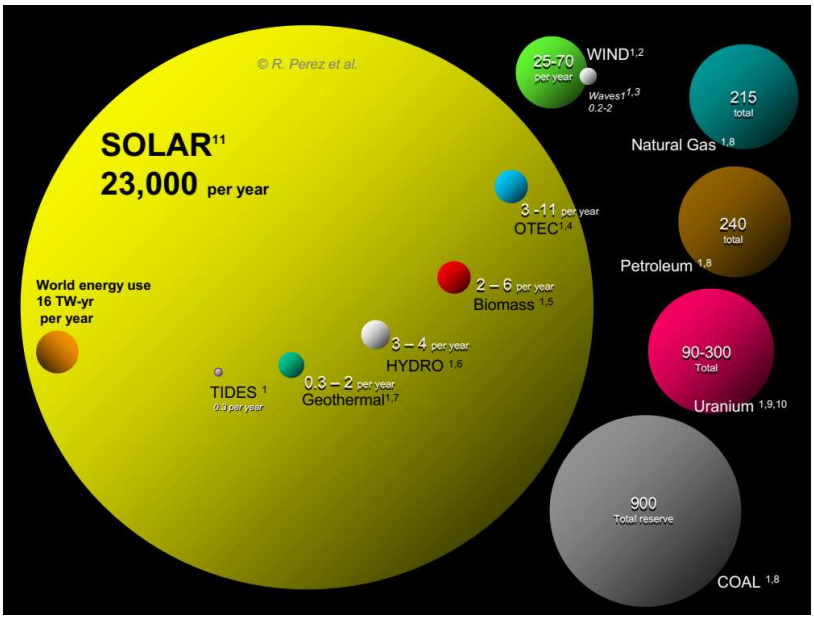

Figure 1-3 The finite and renewable planetary energy reserves comparison [6].

The potential of solar power that can be extracted from solar energy is about 23000 TW/year. This is, over three orders of magnitude higher than total world energy consumption that is about 16 TW/year. Hence, it clearly shows the strong potential of solar energy to fulfill all world energy demands. Wind is the only energy source among all other renewable resources could probably provide the total energy requirements of planet if a significant portion of it can be extractable. Despite the coal reserves are vast, but they wouldn't last more than a few decades if they have been considered as predominant combustion source. Nuclear power isn't a silver bullet which means it can't solve global warming problem by itself. Because it mainly

is used for electricity production which contributes less than 25% of universal greenhouse effects [6, 7].

Figure 1-4 shows, non-renewable energy that had about 73.5% share in global electricity generation by end 2017 and only 26.5% was coming from renewable resources. The largest renewable energy source was belong to hydropower with 16.4% share and solar photovoltaic generated only 1.9% of global electricity production [8].

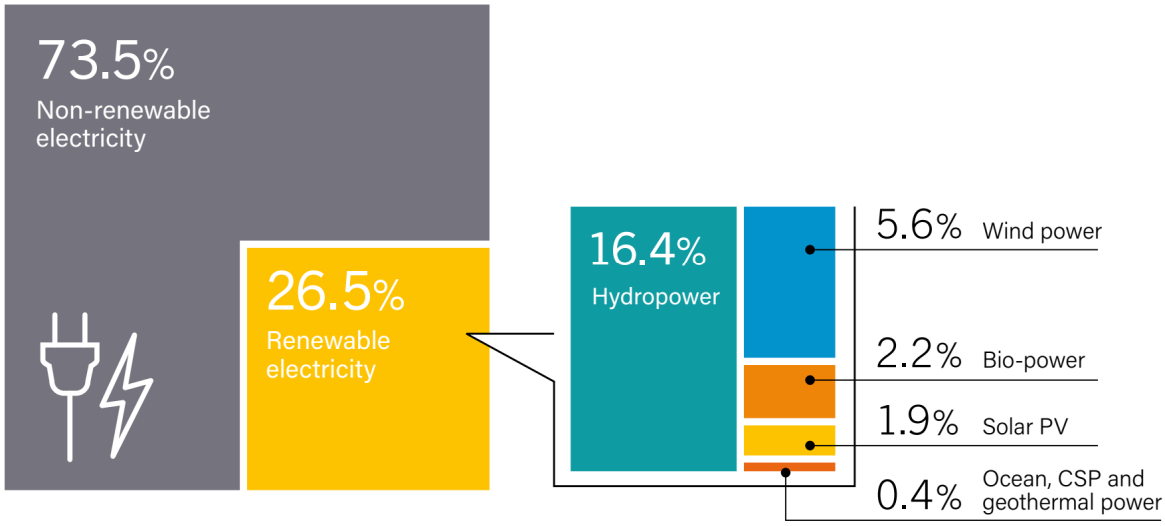

Figure 1-4 Estimated renewable energy share of global electricity production, End-2017 [8].

As we know so far, PV has huge potential to fulfill world energy requirements but still there is no significant tendency to consider it as a predominant source of energy. The main reason could be due to the cost of PV conversion compare to other energy sources that is still high. High cost of solar PV is due to low extraction and power conversion efficiency.

The PV system cost benchmark for different applications has been shown in Figure 1-5 from 2010 to 2017. There is considerable drop in PV cost including module, inventor, hardware components and soft costs in the last few years.

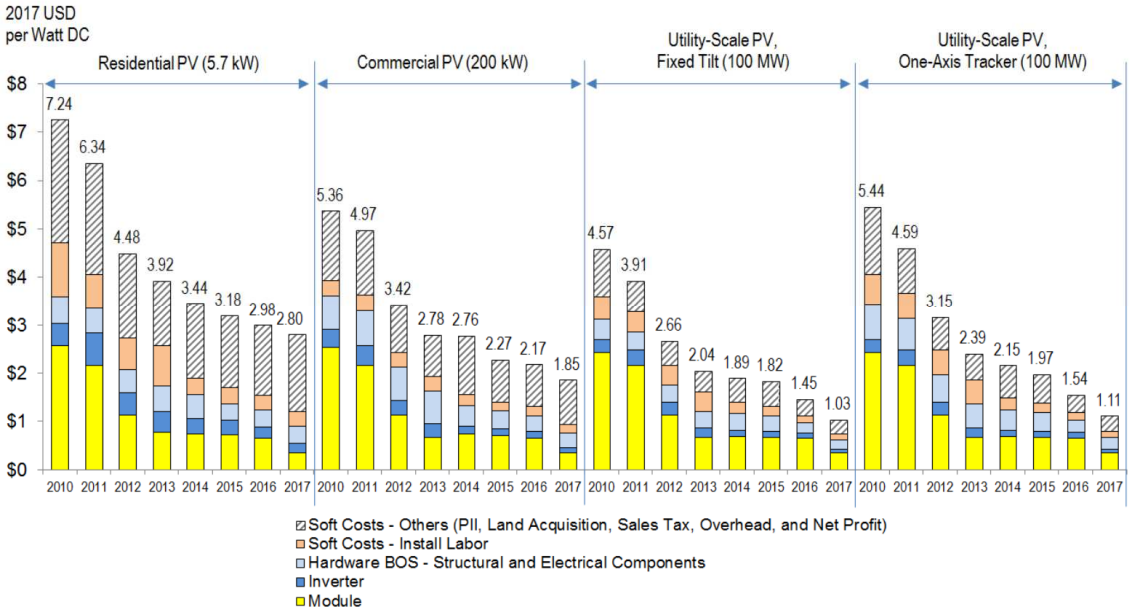

Figure 1-5 NREL PV system cost benchmark summary 2010-2017 [9].

According to US department of energy SunShot institute, the main targets are to reduce the solar technology installed system prices less than $1/watt, $1.25/W, $1.50/W, and $3.60/W for utility-scale, commercial rooftop, residential rooftop, and CSP systems with up to 14 hours of thermal energy storage capacity respectively by end of 2020 [10].

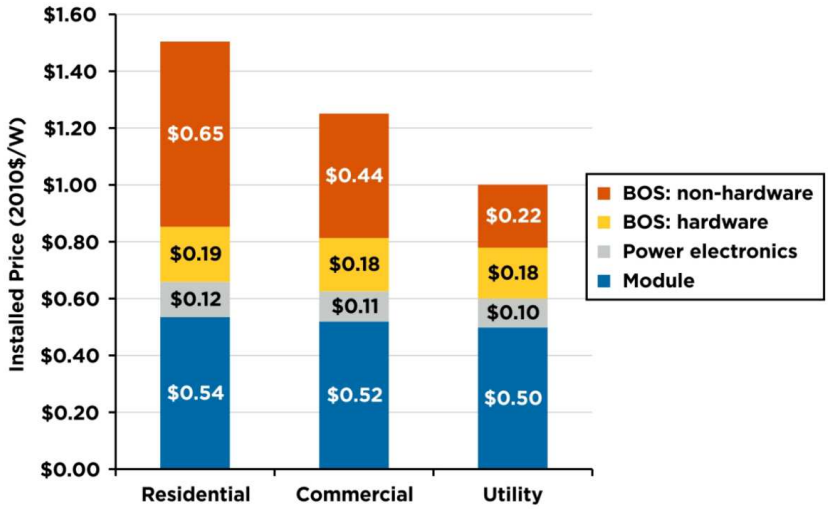

Figure 1-6 Estimated subsystem prices needed to achieve 2020 SunShot targets [10].

1-5 Photovoltaic and Solar Cells

The direct conversion of solar radiation to electric power is called photovoltaic (PV) energy conversion due to PV effect. Photovoltaic effect is refer to generation of voltage across a junction of two different semiconductor materials under illumination of incident light [11].

Solar cell is a semiconductor device which converts solar energy into electricity. A solar cell device is characterized by its conversion efficiency which directly depends on output voltage and current. Solar panel or PV module can be made by connecting a number of solar cells together. Solar panel generates particular voltage or current for specific devices for their operation. Solar array is made by connecting a large number of solar panels to produce large scale electricity (see Figure 1-7) [11].

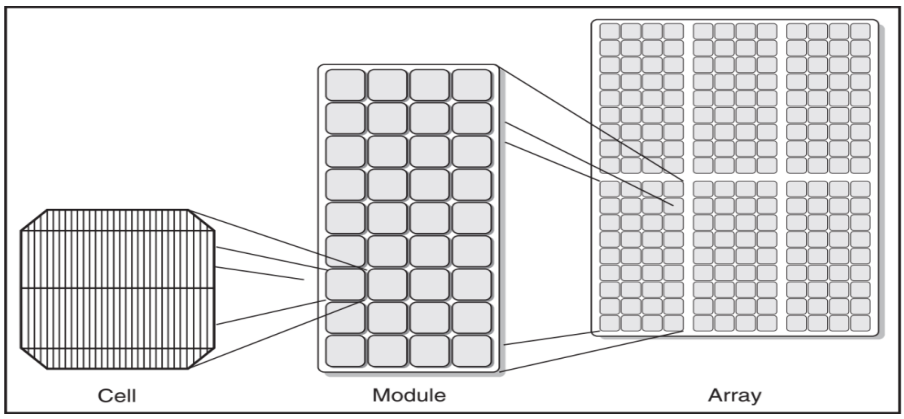

Figure 1-7 Photovoltaic cell, panel (module) and array [12].

Grid connected photovoltaic power system is a solar PV electricity generation system that is connected to power grid. This system require number of charge controllers, batteries, inventors. Inventors, convert direct current (DC) electricity (generated by PV array) into alternative current (AC) electricity because different type of loads such as television, radio and etc. require AC electricity for operation (see Figure 1-8) [12].

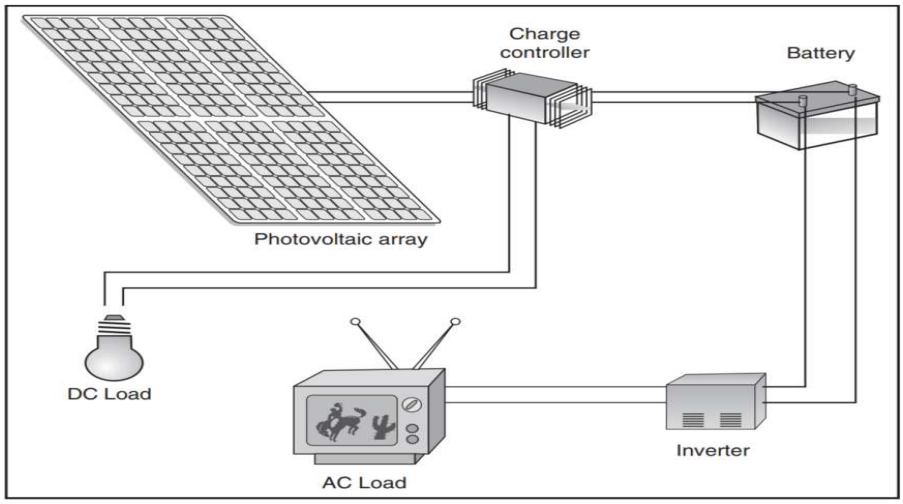

Figure 1-8 Components of a grid connected photovoltaic power system [12].

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CHAPTER 2. DEVICE PHYSICS OF SOLAR CELLS

2-1 Basic structure and working principle of solar cells

Solar cell is a photoelectric device that converts solar radiation into electrical power under photovoltaic effect. Figure 2-1 shows a basic structure of a solar cell from its cross section. Solar cell produces both current and voltage under incident light to generated electrical power.

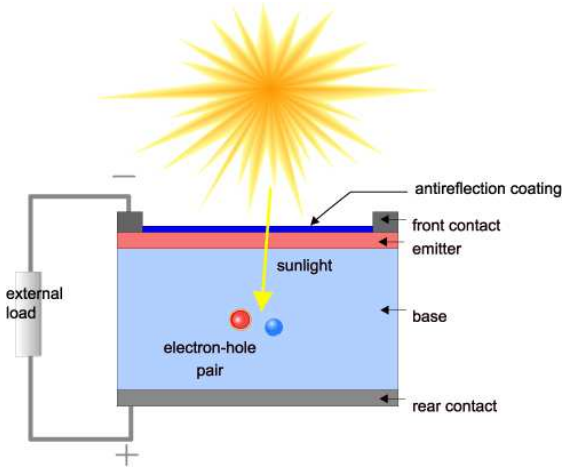

Figure 2-1 Cross section of a solar cell [1].

This process has four main requirements and steps. First, a material with high absorption coefficient which absorbed photons can excite electron from low energy level to high energy level to create electron-hole pairs or excitons. Second, separation of charge carriers to opposite direction. Third, the high energy electron-hole move from solar cell to an external circuit. Finally, returning of electrons and holes to the solar cell after dissipating of their energy in the external load. Although, theoretically many materials should be available to satisfy photovoltaic energy conversion obligations, however in reality the n-type and p-type semiconductor materials mostly are used to make a p-n junction for photovoltaic purposes [1]. The several basic steps in operation of a solar cell have been shown here [1].

- Absorption of incident photons and generation of light-generated electron and hole pairs

- The collection of the light-generated electron and hole pairs to generate a photo current
- The generation of a large electrical voltage across the solar cell p-n junction
- The dissipation of electrical power in the external load and in parasitic resistance

Schematic of a typical single junction silicon solar cell is shown in Figure 2-2. This is a standard n-i-p substrate device which light coming from top (n-side). As we can see, generated electrons and holes are collected using front (finger/bus) and back electrode respectively. Short, medium, and long wavelength photons are absorbed and generated free electron-hole pairs in area close to the surface, in the middle and close to back of the cell respectively. Generated carrier outside and inside depletion regions are transport under diffusion and drift mechanism respectively [2-7].

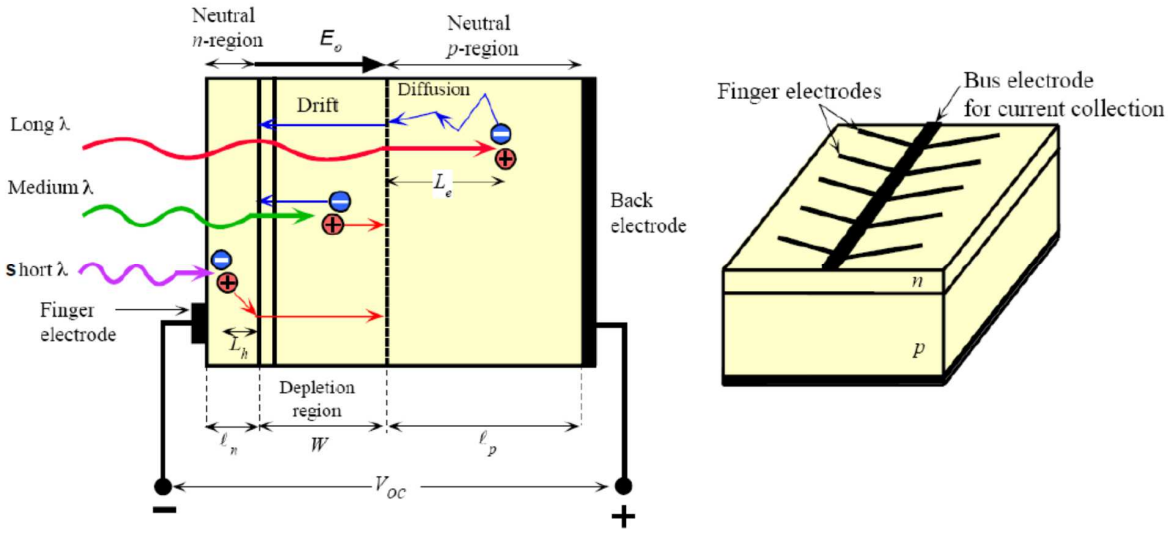

Figure 2-2 Schematic of a typical single junction Silicon solar cell [2-8].

The energy band diagram of a basic PN junction solar cell is shown in Figure 2-3. Photons are absorbed in PN junction depletion region, electrons are collected in N-side and fermi level goes up. Similarly holes are collected in P-side and fermi level moves down. Travel of electrons and holes toward the appropriate contacts can be explained under drift and diffusion

phenomenon which produce photo-current. Open circuit voltage (V_{oc}) is defined by the difference of fermi levels energy in both sides (divided by electron charge).

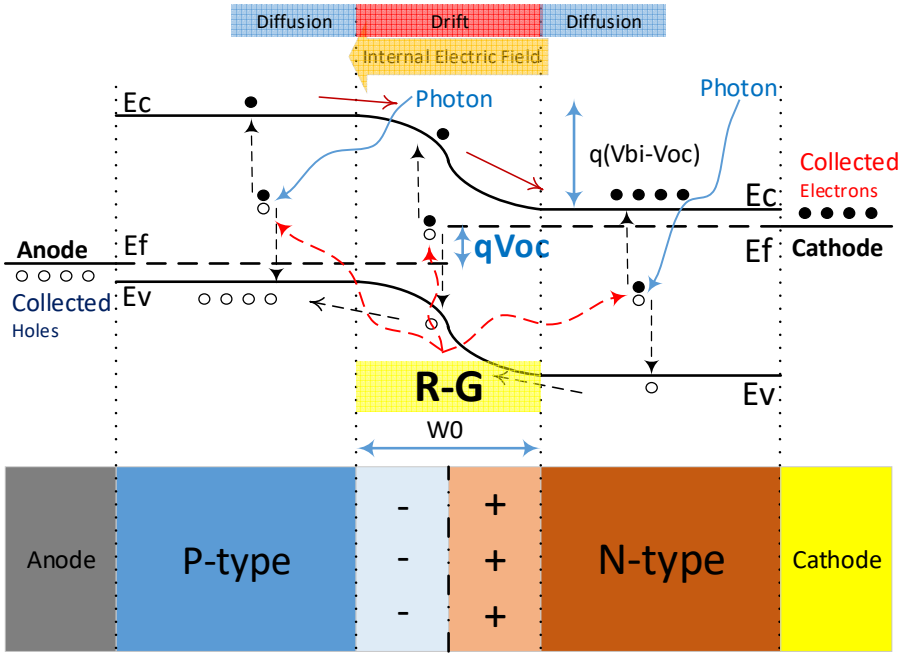

Figure 2-3 Energy band diagram of a silicon PN junction solar cell.

Four basic solar cell device structures have been shown in Figure 2-4 and Figure 2-5. As we can see, a solar cell device consists of a main photo absorbing layer (active layer or i-layer) which has been sandwich between one electron transport layer (ETL) on one side and a hole transport layer (HTL) on another side. Incident photons enter into the solar cell device through a transparent window contact. Photons are absorbed inside the active layer and create electron-hole pairs (EHPs). Electrons and holes are collected by ETL and HTL respectively. Finally, collected carriers generate electrical power in external load.

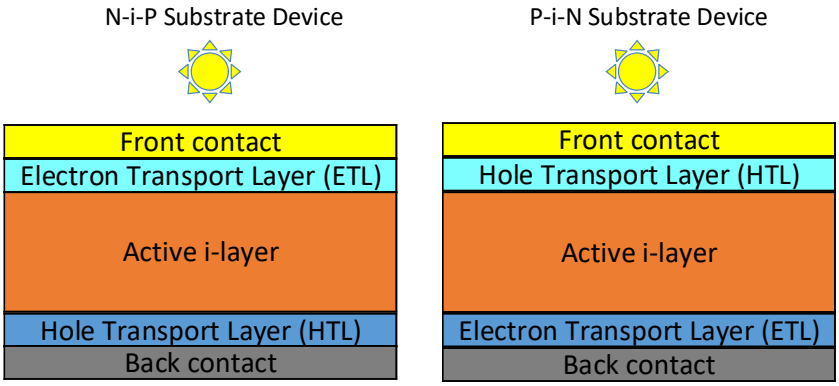

Figure 2-4 Structure of a single junction N-i-P (left) and P-i-N (right) substrate device (Light from top).

For a given device which light coming from the top or bottom, it calls substrate or superstrate device respectively. Also, if light coming from N side or P side, that device has N-i-P and P-i-N structure respectively.

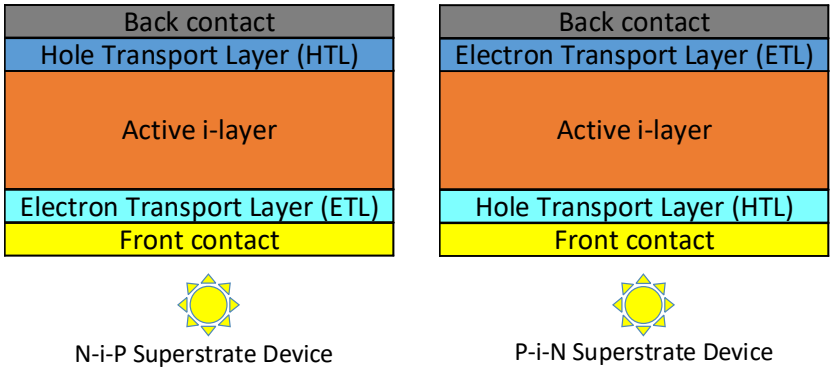

Figure 2-5 Structure of a single junction N-i-P (left) and P-i-N (right) superstrate device (Light from bottom).

Solar cell power conversion efficiency (PCE), is the ratio of device output power over the input power of light source (Sun). PCE is a most important parameter of solar cell which reflects the performance of device and strongly depends on incident light spectrum and temperature. Solar cell for terrestrial applications is measured at 25ºC and under AM1.5 (AM: Air Mass). PCE of a solar cell is depend on several factors such as generation, recombination process and carrier transport.

Generation means, creation of free electron and hole inside the device under absorption of incident light. These free carriers produce photo-current. In order to increase the device efficiency, the generation rate need to be increased.

Recombination means, annihilation of free electrons and holes after generation. Recombination decreases the concentration of free carriers and reduces the device efficiency.

Carrier transport refers to travel of free carriers which have been survived from recombination, toward the device contacts. Carrier transport can be based on electric field or carrier concentration which called drift or diffusion (see Figure 2-6).

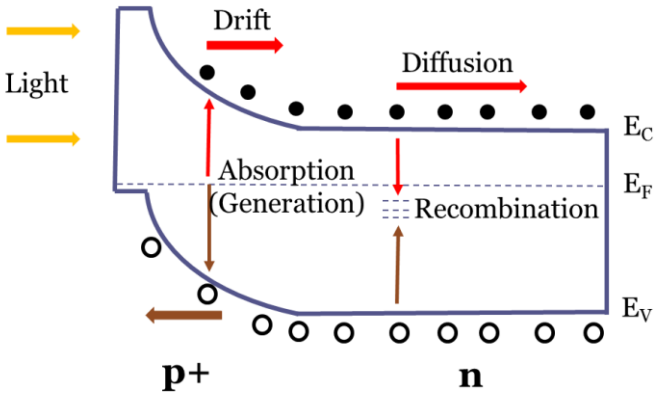

Figure 2-6 Generation, recombination process and carrier transport [3].

2-2 Absorption

The absorption coefficient defines how far light can penetrate into a semiconductor material before it get absorbed. In a material with high absorption, more photons can absorb in distance close to surface which they can excite more electrons into conduction band. On the other hand, light transmits in a material with low absorption if it is thin enough. Characterization of absorption spectrum is a simplest method to analyze the band structure of semiconductors. Through an absorption process, an incident photon with known energy excites an electron to transit from a low energy state to high energy state. Semiconductor materials

have a sharp edge in their absorption coefficient, since only photons with energy higher that band gap are able to be absorbed. Absorption coefficient for various materials is shown here [1].

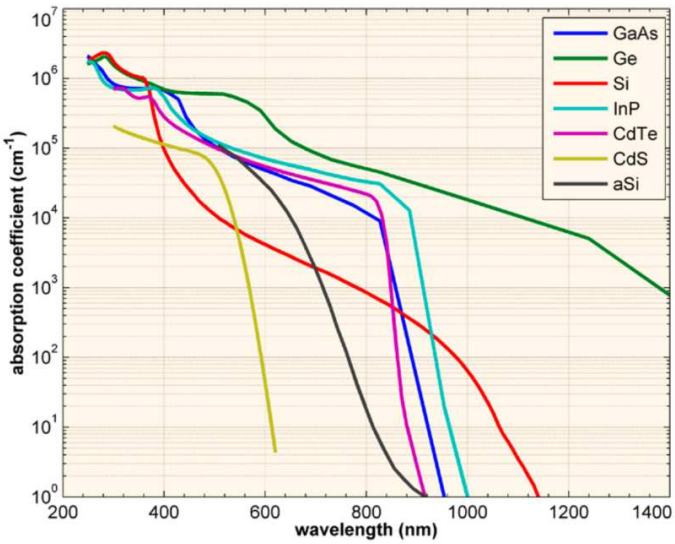

Figure 2-7 the absorption coefficient of different materials as a function of wavelength (nm) [1].

Due to the absorption coefficient of any material, the light intensity exponentially decreases by traveling inside the material. I(x) as light intensity at distance of x from material surface is given by

$$I(x) = I(0)e^{-\alpha x} \tag{2.1}$$

Where I(0) and α are light intensity at x=0 and absorption coefficient respectively.

Study the all possible transitions of an electron is a powerful technique to learn more about the distribution of states in a semiconductor. Some possible transitions could be band-to-band and transition between sub-bands or through defect states. The absorption coefficient α(hν) represents the reduction of light intensity L(hν) vs. its propagation path [5].

$$\alpha(h\nu) = \frac{1}{L(h\nu)} \frac{d[L(h\nu)]}{dx} \tag{2.2}$$

Band-to-band or exciton transition is known as fundamental absorption. This refers to the excitation of an electron form the valance to the conduction band. Fundamental absorption reveals itself by a sharp rise in absorption which also shows the band gap of the semiconductor. A band-to-band allowed direct transition with energy photon higher than bandgap is shown in Figure 2-8. The excess energy of this transition E_{ph}-E_g is dissipated as thermodynamic loss [3, 4].

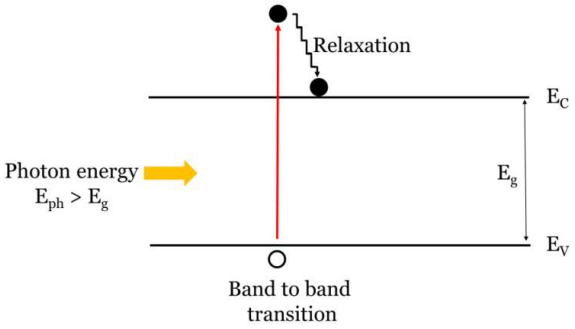

Figure 2-8 Allowed direct band-to-band transition [3].

For the photon energy less than bandgap, the transition can be occurred through mid-gap or tail states. All trap state transitions are achieved within forbidden band is shown in Figure 2-9.

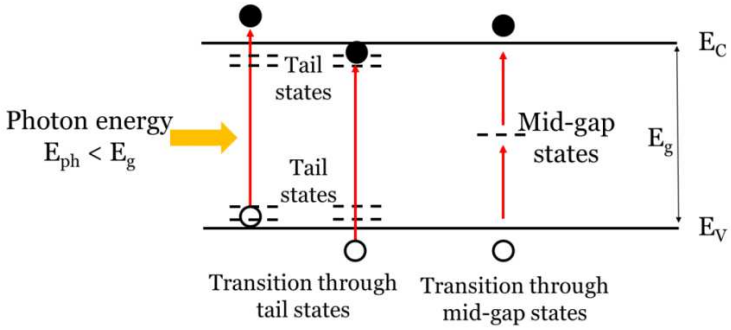

Figure 2-9 Trap state transition within forbidden band [3].

Allowed direct absorption transition occurs between two direct valleys from top of valence bad to bottom of conduction band, see Figure 2-10 (for k=0). Momentum is conserved during this direct transition.

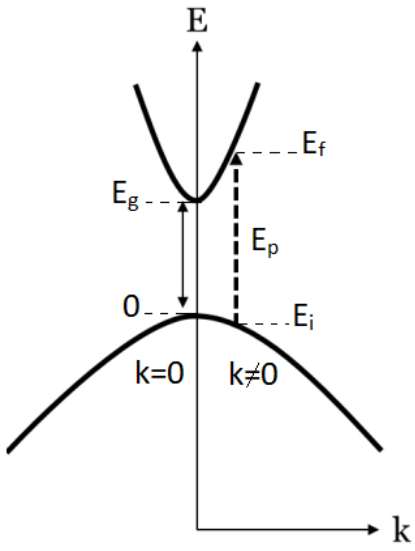

Figure 2-10 Allowed direct transition (k=0) and forbidden direct transition (k≠0) [3, 5].

The absorption coefficient for direct transition is expressed as following equation, where A_0 is given by the effective mass of electron and hole [5].

$$\alpha(h\nu) = A_0\left(h\nu - E_g\right)^{\frac{1}{2}} \tag{2.3}$$

$$A_0 \approx \frac{q^2\left(2\frac{m_h^* m_e^*}{m_h^* + m_e^*}\right)^{3/2}}{nch^2 m_e^*} \tag{2.4}$$

Direct transition isn't allowed in some materials at k = 0 due to quantum selection rules but it allowed at $k \neq 0$ and transition probability increases with k^2 factor. This process is called forbidden direct transitions that is shown in Figure 2-10 (for $k \neq 0$). The absorption coefficient for forbidden direct transition is given by:

$$\alpha(h\nu) = A_1\left(h\nu - E_g\right)^{\frac{3}{2}} \tag{2.5}$$

$$A_1 \approx \frac{4}{3}\frac{q^2\left(2\frac{m_h^* m_e^*}{m_h^*+m_e^*}\right)^{3/2}}{nch^2 m_e^* m_h^* h\nu} \tag{2.6}$$

Indirect transition between two indirect valleys refers to a transition which requires a change in both energy and momentum and it involves two-step process. Photon has zero rest mass and it can't make any change in momentum, but phonon (quantum lattice vibration) interaction, conserves the momentum. Two phonon processes under emission and absorption with phonon's characteristic energy E_p respectively are given by

$$\begin{cases} h\nu_e = E_f - E_i + E_p \\ h\nu_a = E_f - E_i - E_p \end{cases} \tag{2.7}$$

Conservation of momentum via phonon interaction is shown in Figure 2-11.

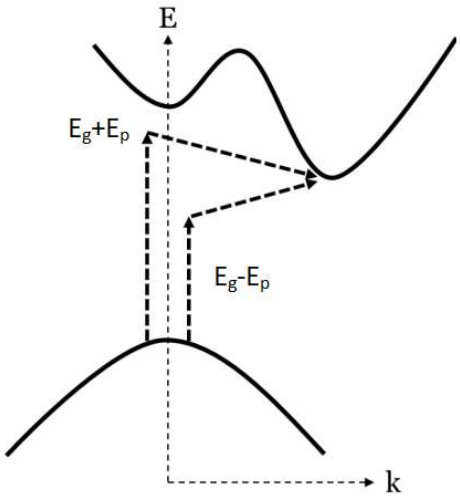

Figure 2-11 Indirect transitions between two indirect valleys [3, 5].

The absorption coefficient through a transition under phonon absorption is given by (2.8) for $h\nu > E_g - E_p$.

$$\alpha_a(h\nu) = \frac{A\left(h\nu - E_g + E_p\right)^2}{\exp\left(\frac{E_p}{kT}\right) - 1} \tag{2.8}$$

Also, the absorption coefficient through a transition under phonon emission is given by (2.9) for $h\nu > E_g + E_p$

$$\alpha_e(h\nu) = \frac{A(h\nu - E_g - E_p)^2}{1 - \exp\left(-\frac{E_p}{kT}\right)} \tag{2.9}$$

In this case, the both phonon emission and absorption are possible and the final equation for absorption coefficient could be

$$\alpha(h\nu) = \alpha_a(h\nu) + \alpha_e(h\nu) \tag{2.10}$$

Figure 2-12 shows how $\alpha_a(h\nu)$ and $\alpha_e(h\nu)$ are related to temperature. According to equation (2.8), $\alpha_a(h\nu)$ is low at very low temperature.

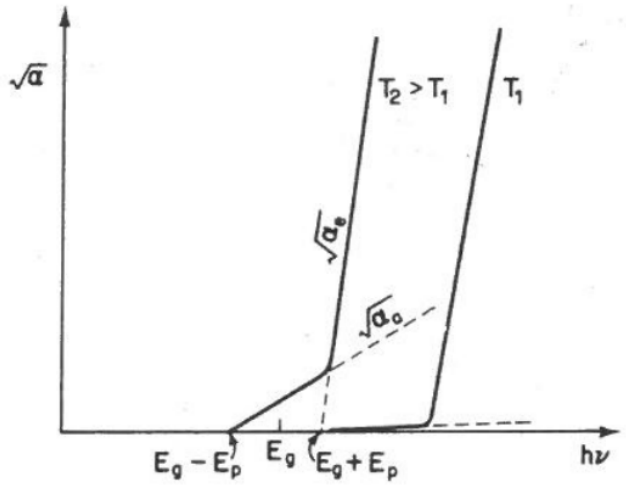

Figure 2-12 Square root of $\alpha(h\nu)$ vs. $h\nu$, gives the values of $E_g - E_p$ and $E_g + E_p$ at $\alpha = 0$ [3].

The density of state for tail and mid-gap state is mainly low. This gives a low absorption coefficient transition and it can be shown by equation (2.11). Where Urbach energy E_u is a function of tail and mid-gap defect states [3, 6].

$$\alpha = Ae^{\frac{h\nu}{E_u}} \tag{2.11}$$

2-3 Recombination

As we mentioned before, recombination is a process which both electrons and holes annihilate each other. Both carriers disappear finally under recombination and energy difference between two initial and final energy states release inform of radiative recombination (photons or light) or non-radiative recombination (phonons or heat). This chapter includes five main categories of recombination. Supplemental explanation on band-to-band, center, shallow levels, excitons and auger recombination will be provided in following parts [6].

2-3-1 Band-to-band recombination

Band-to-band recombination refers to radiative recombination which involves a direct annihilation of an electron from conduction band with a hole in valance band (see Figure 2-13). During radiative recombination process, excess energy releases inform of photon or light.

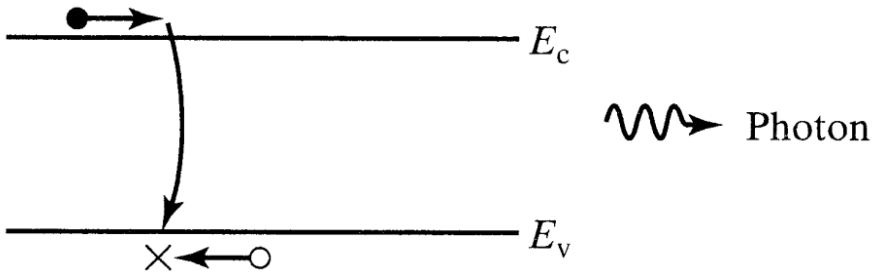

Figure 2-13 Band-to-band recombination [7].

Band-to-band recombination rate (R) could be shown by:

$$R = C_B(np - n_i^2) \tag{2.12}$$

Where C_B is the recombination coefficient, n, p, and n_i are electron, hole, and intrinsic carrier concentration respectively.

Under small signal (SS) case:

Low level charge injection: $\Delta n, \Delta p << n$

n-type material: $n >> p$ and $n >> n_i$

We can re-write equation into

$$R = C_B n \Delta p = \frac{\Delta p}{1/C_B n} = \frac{\Delta p}{\tau_B} \tag{2.13}$$

Where $\tau_B = 1/C_B n$ is the minority lifetime.

Under large signal (LS) case:

High level charge injection $\Delta n, \Delta p >> n_0, p_0$

Simplified equation for this case would be

$$R = C_B \Delta n \Delta p = C_B np = C_B n^2 = C_B p^2 \tag{2.14}$$

2-3-2 Trap-assisted or schottky read hall (SRH) recombination

Crystalline solid materials, express a periodic, well arrangement of molecules and atoms next together. However this crystalline structure can be interrupted by defects, missing atoms or impurities. Defects in semiconductor can occur in several different forms like point, line, planar and bulk defects which introduce midgap energy levels (E_T). Crystal defects increase deep-level states. Trap-assisted or SRH recombination refers to non-radiative process which an electron from conduction band and a hole from valance recombine, annihilate inside the midgap state. During non-radiative process, excess energy releases inform of phonons or heat (see Figure 2-14) [7].

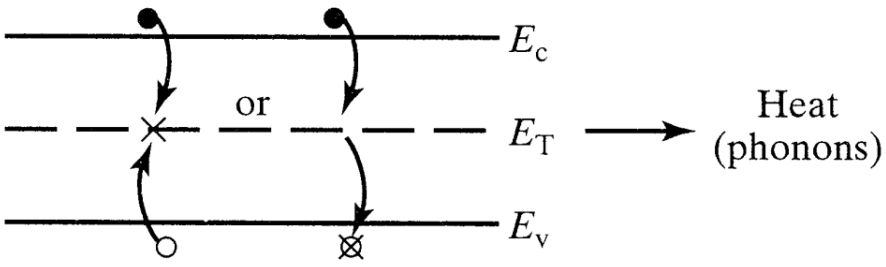

Figure 2-14 R-G center recombination [7].

For trap-assisted recombination rate we can write:

$$R = \frac{np - n_i^2}{\tau_p(n + n_1) + \tau_n(p + p_1)} \tag{2.15}$$

Where τ_n and τ_p are electrons and holes minority carrier lifetime which depends on defect density N_T.

$$\tau_n = \frac{1}{c_n N_T} \text{ and } \tau_p = \frac{1}{c_p N_T} \tag{2.16}$$

Here n_1 and p_1 are computable constants which can be expressed by following equation [7].

$$n_1 = n_i \exp\left(\frac{E_T - E_i}{kT}\right) \quad \text{and} \quad p_1 = n_i \exp\left(\frac{E_i - E_T}{kT}\right) \tag{2.17}$$

$$n_1 p_1 = n_i^2 \tag{2.18}$$

Under small signal (SS) case:

Low level charge injection: Δn, $\Delta p << n$

n-type material:

$$R = C_n \Delta n N_T = \frac{\Delta n}{\tau_n} \tag{2.19}$$

p-type material:

$$R = C_p \Delta p N_T = \frac{\Delta p}{\tau_p} \tag{2.20}$$

Hence, SRH recombination rate is proportional the defect density (N_T)

Under large signal (LS) case:

High level charge injection: Δn, $\Delta p >> n_0$, and p_0

$$R = \frac{\Delta n}{\tau_n + \tau_p} = \frac{\Delta p}{\tau_n + \tau_p} \tag{2.21}$$

Where, τ is effective lifetime in SRH recombination.

$$\tau = \tau_n + \tau_p \tag{2.22}$$

2-3-3 Auger recombination

Auger (pronounced Oh-jay) recombination refers to a non-radiative process involving three carriers. In an Auger process, a band-to-band or trap-assisted recombination occurs simultaneously, one electron from conduction band recombine with one hole from valance band. The energy released from this process, excites the third carrier (mainly electron) to high energy level. Finally, this high energetic carrier, loses its energy gradually under lattice collisions (see Figure 2-15). Auger recombination is dominant in degenerate semiconductor and under high carrier concentration.

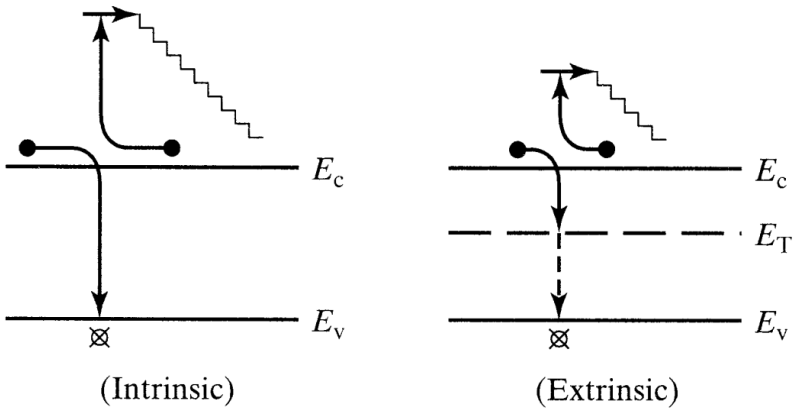

Figure 2-15 Auger recombination [7].

Auger recombination rate is defined by

Under small signal (SS) case:

Low level charge injection: Δn, Δp << n

n-type material:

$$R = C_A n(np - n_i^2) \tag{2.23}$$

$$R = C_A n_0^2 \Delta p = \frac{\Delta p}{1/C_A n_0^2} = \frac{\Delta p}{\tau_p} \tag{2.24}$$

$$\tau_p = \frac{1}{C_A n_0^2} \tag{2.25}$$

p-type material:

$$R = C_A p(np - n_i^2) \tag{2.26}$$

$$R = C_A n_0^2 \Delta n = \frac{\Delta n}{1/C_A n_0^2} = \frac{\Delta n}{\tau_n} \tag{2.27}$$

$$\tau_n = \frac{1}{C_A n_0^2} \tag{2.28}$$

Auger recombination rate is directly proportional to the square of carrier concentration. The overall recombination life time in a semiconductor is the superposition of all three recombination life time which have been discussed above, therefore it would be:

$$\frac{1}{\tau_{Overal}} = \frac{1}{\tau_{Band-to-band}} + \frac{1}{\tau_{Trap-assisted}} + \frac{1}{\tau_{Auger}} \tag{2.29}$$

2-3-4 Recombination through Shallow Levels

Shallow level sites which are close to conduction (donor site) and also valance bands (acceptor site) play a critical role to induce the carriers to recombine. The recombination probability for those electrons and holes which are captured at donor and acceptor sites respectively are so low. Because the probability of those carriers to re-emit into their original energy states at room temperature before completing the recombination process is high. Shallow level recombination is mostly radiative process and system temperature reduction improves the recombination probability [7].

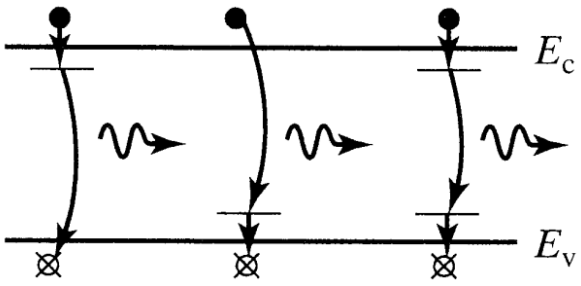

Figure 2-16 Recombination through shallow levels [7].

2-3-5 Recombination involving excitons

The coupled electron-hole pair under Coulombic force which are not free carriers is called Exciton. Electron and hole in form of Exciton are bounded together into hydrogen atom arrangement and moves as a single unit under external applied force. A certain amount of energy is needed to formation of Exciton at a shallow-level site is called binding energy E_b. Exciton's binding energy as the energy difference between electron and hole is less than bandgap due to Coulombic attraction. Figure 2-17 shows the Exciton formation takes place inside the bandgap, slightly below of conduction or slightly above the valence band. Exciton sites are shown by parentheses. Exciton recombination is very dominant at low temperature and it plays a major role in light-generation mechanism in Light Emitting Diodes (LEDs) [6].

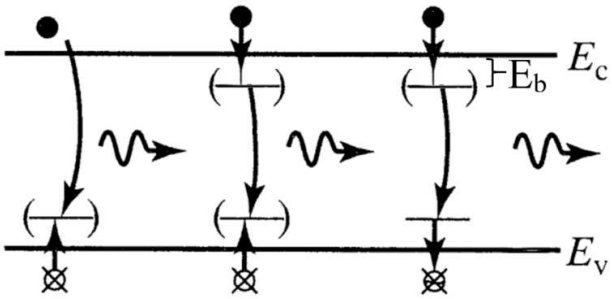

Figure 2-17 Recombination involving excitons [7].

The Exciton binding energy can be expressed by [4, 9]

$$E_b = -\frac{\mu R_H}{m_0 \varepsilon_r n^2} \tag{2.30}$$

μ: reduced mass

m_0: free electron mass

R_H: Rydberg constant of hydrogen atom (=13.6 eV)

ϵ_r: Dielectric constant of the material

n: level of binding energy

2-4 Carrier collection

Collection of light-generated carriers is of the main steps in operation of a solar cell which is controlled under drift and diffusion mechanisms. Charge carriers transport under drift and diffusion phenomena within a semiconductor. Drift-based transport takes place under internal electric field while diffusion based-transport is relied on gradient of carrier concentration inside semiconductor materials [3, 4, 7, 9-11].

The charge transport equation by considering both drift and diffusion transports could follow by:

$$D' \frac{\partial^2(\Delta n)}{\partial x^2} + \mu' \varepsilon \frac{\partial(\Delta n)}{\partial x} + G - R = \frac{\partial(\Delta n)}{\partial t} \tag{2.31}$$

Where

Δn: The excess electron concentration.

ε: The electric field.

G and R, are generation and recombination rate respectively.

D': The ambipolar diffusion coefficient which is expressed by:

$$D' = \frac{n\mu_n D_p + p\mu_p D_n}{n\mu_n + p\mu_p} \tag{2.32}$$

μ': The ambipolar mobility which can be shown by:

$$\mu' = \frac{\mu_n \mu_p (p - n)}{n\mu_n + p\mu_p} \tag{2.33}$$

μ_n and μ_p are electron and hole mobility respectively.

D_n and D_p are diffusion coefficient for electron and hole respectively.

The ambipolar equation, for n-type semiconductor at low level injection is expressed by substituting $R = \Delta p/\tau_p$:

$$D_p \frac{\partial^2(\Delta p)}{\partial x^2} - \mu_p \varepsilon \frac{\partial(\Delta p)}{\partial x} + G - \frac{\Delta p}{\tau_p} = \frac{\partial(\Delta p)}{\partial t} \tag{2.34}$$

In the same way, the ambipolar equation, for p-type semiconductor at low level injection is shown by substituting $R = \Delta n/\tau_n$:

$$D_n \frac{\partial^2(\Delta n)}{\partial x^2} + \mu_n \varepsilon \frac{\partial(\Delta n)}{\partial x} + G - \frac{\Delta n}{\tau_n} = \frac{\partial(\Delta n)}{\partial t} \tag{2.35}$$

Two above equations show that, minority carriers have major role in the transport process in photovoltaic devices.

2-4-1 Diffusion based collection

Diffusion is refer to particles transport from a region with higher carrier concentration into a region with lower concentration due to their random thermal energy. A simple visualization of particles diffusion in microscopic scale is shown in Figure 2-18 (a). It clearly shows the equal number of particles are moving in both sides (-x and +x directions). On the other hand, the microscopic visualization purely shows the direction of particles diffusion from high concentration area to low concentration region (see Figure 2-18(b)).

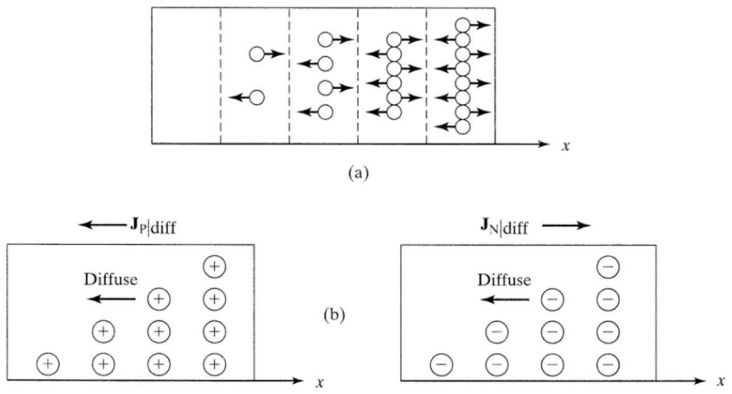

Figure 2-18 Particle diffusion on a microscopic scale (Top), Hole and electron diffusion in macroscopic scale (Bottom) [7].

The ambipolar equation for p-type semiconductor at steady state $\partial(\Delta n)/\partial t = 0$ by assuming no charge generation $G = 0$ and no electric field $\varepsilon = 0$ is reduced to:

$$D_n \frac{\partial^2(\Delta n)}{\partial x^2} = \frac{\Delta n}{\tau_n} \tag{2.36}$$

As a result, the carrier concentration pursues an exponential distribution, where $L_n = \sqrt{(D_n \tau_n)}$ is the electron diffusion length.

$$\Delta n(x) = \Delta n(0) \exp\left(-\frac{x}{L_n}\right) \tag{2.37}$$

Minority carrier diffusion length is one of the main parameter to design solar cell and it should be large enough (comparable with device thickness), so carriers could diffuse through the whole sample thickness and reach the contacts.

2-4-2 Drift assisted collection

The motion of charged-particles under an applied electric field is called drift. The visualization of carriers drift in a semiconductor is shown in Figure 2-19. Applied electric field (E) across the materials, forces and accelerates the positive charges (+q, as hole) and negative charges (-q, as electron) in the same and opposite direction of electric field respectively.

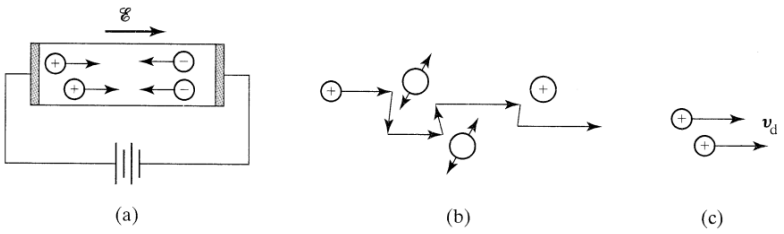

Figure 2-19 The visualization of carrier drift [7]

Carrier motion is repeatedly interrupted due to many scattering events or collisions with ionizes impurity atoms. The net microscopic carrier drift movement is kind of complex as shown in Figure 2-19 (b). But the average transport of the carriers drift in macroscopic scale is observable (see Figure 2-19, (b)).

Drift assisted collection is so important in solar cell with low diffusion length like amorphous silicon cell. Because the charge collection is low due to poor diffusion length, in this case we

need electric field to boost carrier's collection. Figure 2-20 shows a p-i-n amorphous solar cell, which an intrinsic amorphous silicon (i-a-Si) is sandwiched between a p^+ layer and n^+ layer. Due to the internal electric field, generated electrons (filled black circles) and holes (empty circles) move toward the n^+ layer and p^+ layer respectively.

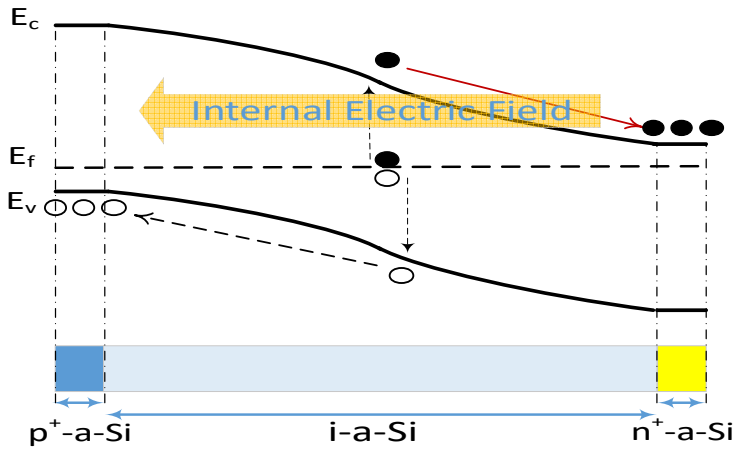

Figure 2-20 p-i-n amorphous silicon solar cell structure, Internal electric field form n^+ layer toward p^+ layer.

Now, let's consider p-type semiconductor and see effect of electric filed. So we can ignore diffusion part ($D_n = 0$), of course no charge generation G = 0.

$$\frac{\partial(\Delta n)}{\partial t} = \mu_n \varepsilon \frac{\partial(\Delta n)}{\partial x} - \frac{\Delta n}{\tau_n} \tag{2.38}$$

The solution gives an exponential distribution for carrier concentration, where $R_n = \mu_n \tau_n$ is the drift range of minority electrons.

$$\Delta n(x) = \Delta n(0) \exp\left(-\frac{x}{R_p}\right) \tag{2.39}$$

A critical electric field E_c is defined at the present of both drift and diffusion based collection

$$E_c = \frac{kT}{qL_p} \tag{2.40}$$

Where for $E > E_c$ then drift-based transport is dominated and for $E < E_c$ diffusion-based transport is dominated [12].

2-5 The Shockley-Queisser limit

The Shockley-Queisser (SQ) limit or detailed balance limit is refers to theoretical calculation to derive maximum power efficiency for a single pn junction solar cell by William Shockley and Hans Queisser [13]. The maximum efficiency as a function of bandgap for a single pn junction is shown in Figure 2-21, the calculation shows the maximum theoretical efficiency is equal to 33.7% under one sun (AM 1.5) of solar spectrum (6000K blackbody radiation).

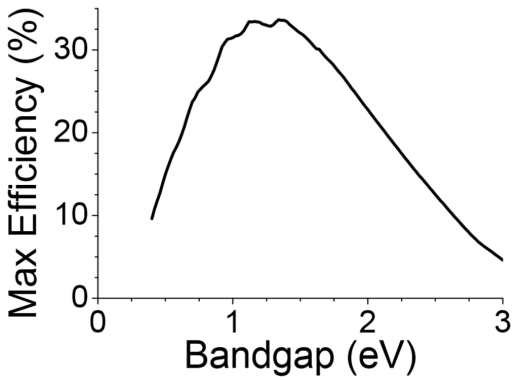

Figure 2-21 Shockley-Queisser (SQ) Limit shows the maximum efficiency is about 33.7% around 1.34eV [13, 14].

Three main assumptions in SQ limit concept are blackbody radiation, recombination and spectrum losses.

Blackbody radiation: When a solar cell is illuminated under the sunlight, any inefficiency in the device turns into heat and increases the cell temperature. As the cell temperature increases, the blackbody radiation also increases. Energy loss due to blackbody radiation term means, the black body radiation from a solar cell at room temperature (RT: 300K) or at higher temperature cannot be captured by cell. This loss is about 7% of incoming energy at RT and even more at higher temperature.

Recombination: Theoretical performance of silicon solar cell is reduced by 10% due to electron-hole pair recombination by effecting the open circuit (V_{oc}) voltage. As it shown in Figure 2-22(A), the red dotted line is $V_{oc} = E_g$ and black line is an upper limit for V_{oc} according to SQ limit.

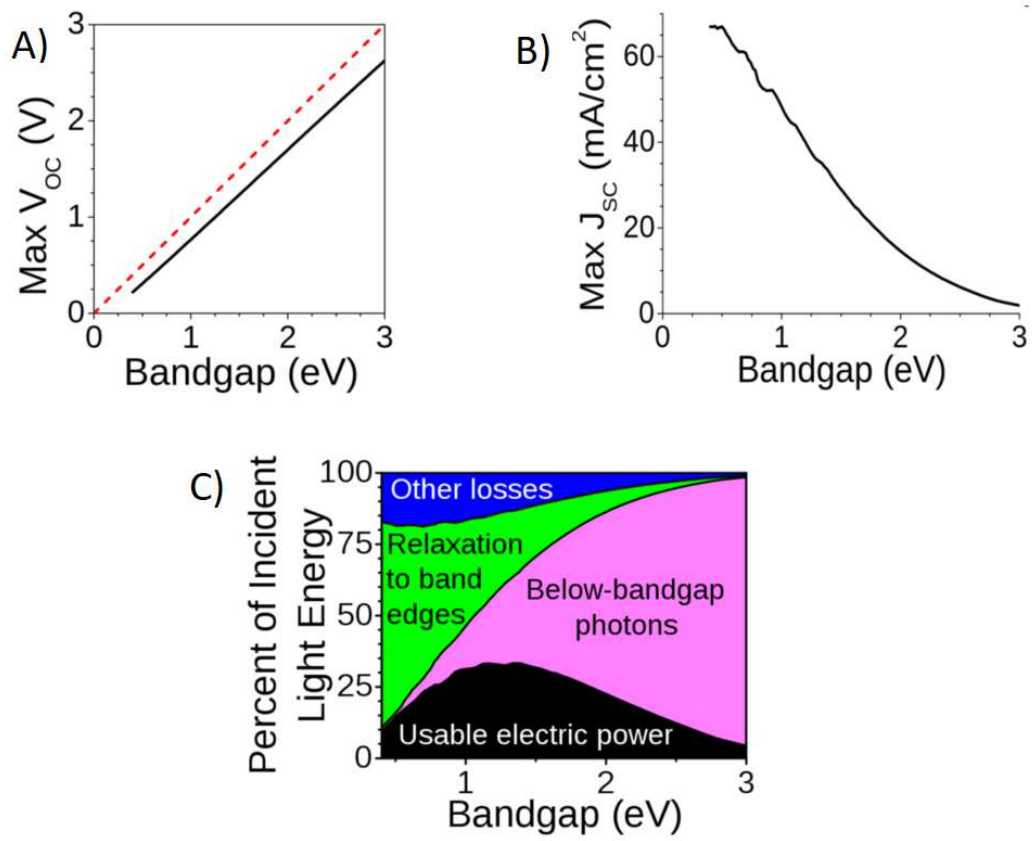

Figure 2-22 Main considerations for the Shockley-Queisser limit. Open circuit voltage (A), short circuit current desity (B), usable and lost energy (C) as a function of material bandgap. [13, 14].

Spectrum loss: Spectrum loss means, for high bandgap materials there are a few photons with energy above the bandgap. This fact put a limit for short-circuit current density (see Figure 2-22 (B)).

Figure 2-22 (C) shows the usable electric power (black area) for the Shockley-Queisser limit and energy corresponding to bellow-bandgap photons (pink height). Also some energy lost due to hot photo-generated carrier's relaxation into the band edges (green height).

2-6 References

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CHAPTER 3. DEVICE CHARACTERIZATION TECHNIQUES OF SOLAR CELLS

3-1 Introduction

In this chapter we will discuss different measurement techniques to characterize the physical, optical, and electronic properties of semiconductor materials and devices. This helps to understand the operational mechanism, also troubleshoot the problems of the photovoltaic devices.

3-2 Solar cell equivalent circuit

The equivalent circuit of a solar cell with single diode is shown in Figure 3-1. I_L is light generate current in parallel with the single diode as I_D. R_{Sh} and R_S are the parasitic shunt and series resistances respectively.

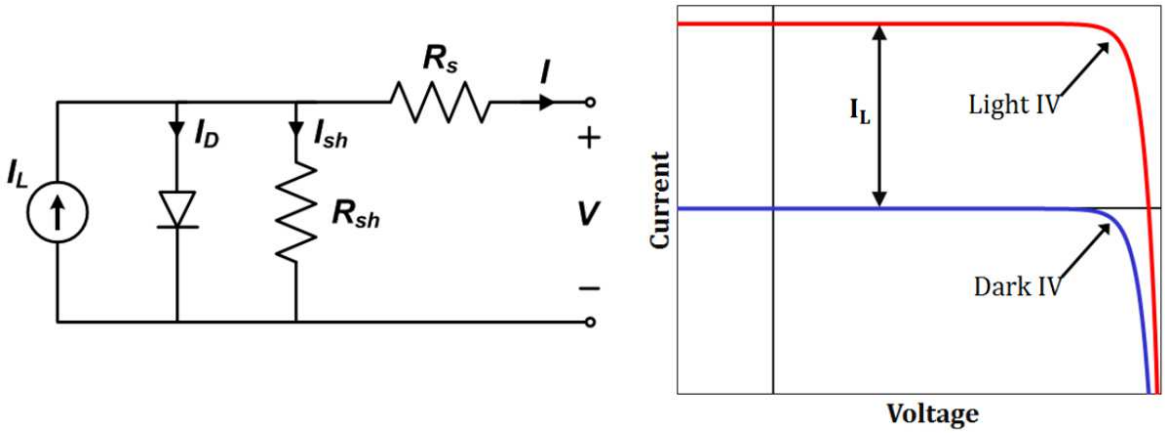

Figure 3-1 Equivalent circuit of a single diode model solar cell (Left), Light and dark (IV) characterization for ideal device (Right) [1, 2].

The total extracted current (I) from the solar cell through the external load is given by:

$$I = I_L - I_D - I_{Sh} \tag{3.1}$$

Where, I_L, I_D, and I_{Sh} are photo-generated current, diode current and shunt current. Diode current is given by:

$$I_D = I_0 \left[\exp\left(\frac{qV}{nkT}\right) - 1\right] \quad (3.2)$$

Where I_0 is reverse saturation current, n is ideality factor (normally between 1 and 2), and V is applied voltage across the device. (V_T = kT as thermal voltage is equal to 25.9 mV at 300°K).

Finally, by substituting (3.2) in (3.1), the final solar cell current can be given by following equation:

$$I = I_L - I_0 \left[\exp\left(\frac{qV}{nkT}\right) - 1\right] - \frac{V + IR_s}{R_{sh}} \quad (3.3)$$

The dark and light current curves versus voltage are shown in Figure 3-1 (Right) for an ideal solar cell where R_S and R_{Sh} are equal to zero and infinity respectively.

In practice, two ideality factors are needed to accommodate I-V curve under applied voltage, also it helps to explain different recombination phenomenon in a solar cell. The double-diode model equivalent circuit of a solar cell is shown in Figure 3-2.

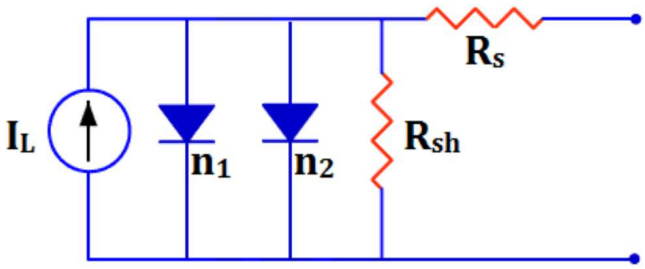

Figure 3-2 Double-diode model equivalent circuit of a solar cell under light [3].

The current equation of the double-diode model under illumination is given by:

$$I = I_L - I_{Dark} \quad (3.4)$$

Where, I_{Dark} is the current equation of the double-diode model [3]:

$$I_{Dark} = I_{01}\left[\exp\left(\frac{q(V + IR_s)}{n_1 kT}\right) - 1\right] + I_{02}\left[\exp\left(\frac{q(V + IR_s)}{n_2 kT}\right) - 1\right] + \frac{V + IR_s}{R_{shunt}} \quad (3.5)$$

Where, $n_1 = 1$ and $n_2 = 2$ are ideality factors, and I_{01} and I_{02} are reverse saturation currents for first and second diode respectively.

3-3 Current-Voltage (IV) measurement of solar cell

One of the most basic and fundamental solar cell characterization techniques is the IV measurement. This is a standard testing that provides many technical device parameters such as open circuit voltage (V_{oc}), short circuit current (I_{sc}), fill factor (FF), efficiency (η), series resistance (R_s), and shunt resistance (R_{Sh}). A basic IV measurement setup for solar cell devices is shown in Figure 3-3 [4]. As it is shown in the schematic, in order to overcome contact resistance problems, current and voltage are measured separately using four point probe technique. IV testing can be performed either under light (Light IV) or in dark (Dark IV).

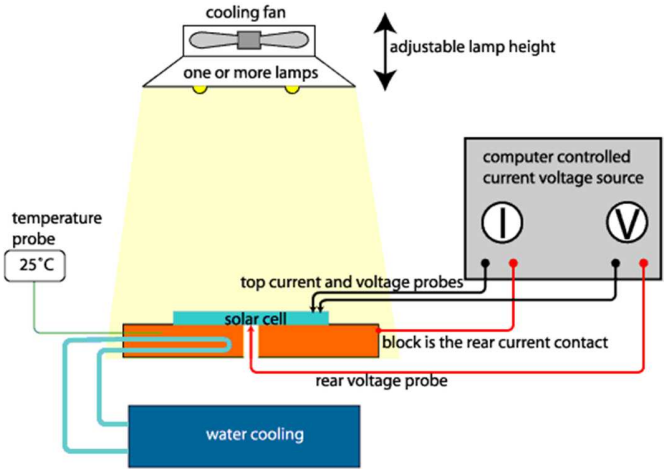

Figure 3-3 A basis IV measurement setup for solar cell [4].

The basic standards required to design a solar cell testing system are listed below [4]:

- Air mass 1.5 (AM1.5) and Air mass 0 (AM0) spectrum respectively for terrestrial and space cells.
- Simulated light source intensity of 100 mW/cm^2 that is known as one-sun of illumination
- Cooling system (using a fan) to keep cell temperature about 25°C during measurement
- Four-point probe to measure IV

Four-point probe supplies a current through the outer two probes using a high impedance current source and measures the voltage across the inner two probes using a voltmeter. FPP helps to remove the effect of probe-cell contact resistance.

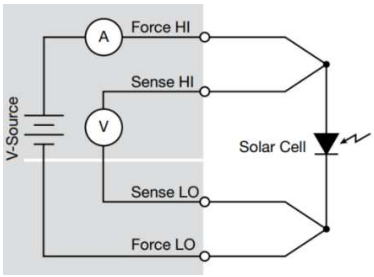

Figure 3-4 Four-point probe connection to a solar cell for IV measurement [5].

Another technique to measure IV, where current is measured while voltage is applied across the device for a desirable ranges (0V to 15% of V_{oc}) (see Figure 3-5).

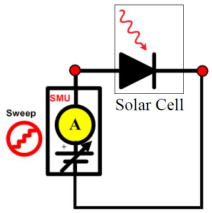

Figure 3-5 Two probes connection to a solar cell for I-V measurement [6].

3-3-1 Light I-V measurement

As it mentioned before, current-voltage (I-V) measurement can provide many parameters of the solar cell which the idealized equivalent circuit model is shown in Figure 3-6.

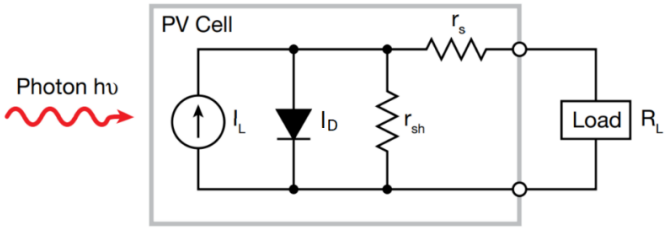

Figure 3-6 Idealized equivalent circuit of a photovoltaic cell [6].

Where, I_L is the light-induced current source, I_D is a diode that generates a saturation current. R_S and R_{Sh} are series and shunt resistance respectively. R_L is the load resistor connected to an illuminated solar cell. A typical forward I-V characteristics of photovoltaic cell is represented in Figure 3-7.

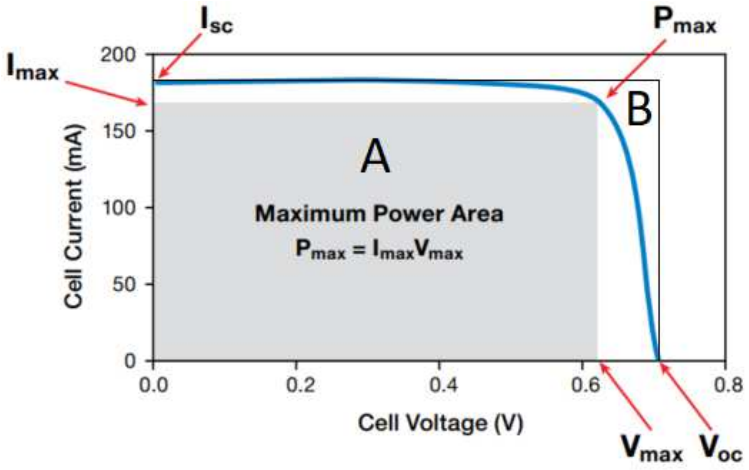

Figure 3-7 Typical forward I-V characteristics of photovoltaic cell [3-5].

Several parameters are used to characterize the solar cell which are illustrated in Figure 3-7. The open-circuit voltage V_{oc} gives the voltage at zero current. The short-circuit I_{sc} provides the current at zero voltage.

The open-circuit voltage can be express by the following equation:

$$V_{oc} = \frac{nkT}{q} \ln\left(\frac{I_L}{I_0} + 1\right) \tag{3.6}$$

The short-circuit current is given by the following equation:

$$I_{sc} = qAG(L_n + L_p) \tag{3.7}$$

Where, q is electron charge, A is device area, G is generation rate, L_n and L_p are electron and hole diffusion length respectively.

The maximum power ($P_{max} = V_{max} \times I_{max}$) is the product of the current and voltage where the output power is greatest. As we mentioned previously for terrestrial application, solar cell is

measured under one-sun (AM1.5) of illumination which is correspond to input power P_{in} = 100 mW/cm^2 of light intensity.

The fill factor (FF) is critical parameter to define how far the I-V characteristics of an actual photovoltaic cell differ from the ideal cell. The fill factor for an ideal solar cell will be equal to one (1) but losses due to series and shunt resistances for a practical solar cell always make it lower than one. The fill factor can be defined as the ratio between maximum power to the product of open-circuit voltage and short-circuit current.

$$FF = \frac{Area\_A}{Area\_B} = \frac{V_{max}\, I_{max}}{V_{oc}\, I_{sc}} \tag{3.8}$$

Where, I_{max} and V_{max} are the current and voltage at the maximum output power. Solar cell conversion efficiency (η) refers to ratio of solar energy that can be converted into electrical power.

$$\text{Efficiency} = \eta = \frac{P_{max}}{P_{in}} = \frac{V_{oc} \times I_{sc} \times FF}{P_{in}} \tag{3.9}$$

The impact of both series and shunt resistances is shown in Figure 3-8. The series resistance is mainly due to the resistance or losses of the metal and ohmic contact in the front and back surfaces of the device, junction depth, and impurity concentrations. The series resistance is an important parameter because low series resistance increases the device short-circuit current that can maximize the output power. In the ideal case, the series resistance is equal to zero (R_{Series} = 0). On the other hand, the shunt resistance is due to surface leakage loss along the edge of the device or crystal defects. In the ideal case, the shunt resistance is equal to infinite (R_{Shunt} = ∞) [5, 7].

$$R_{Shunt} = \left.\frac{\partial V}{\partial I}\right|_{V=0} \tag{3.10}$$

$$R_{Series} = \left.\frac{\partial V}{\partial I}\right|_{V=V_{oc}} \tag{3.11}$$

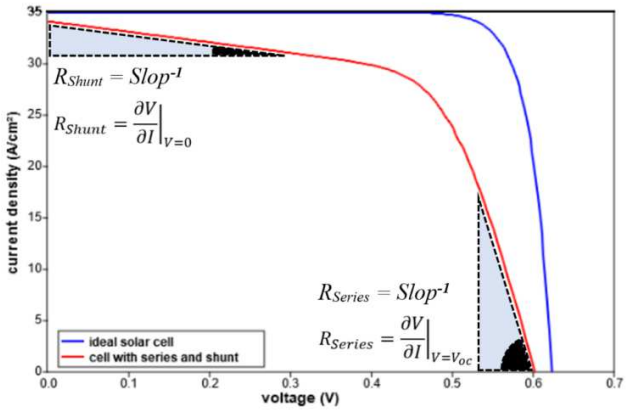

Figure 3-8 Light I-V characteristics of a photovoltaic cell, Ideal cell (Blue), Practical Cell (Red) [7].

3-3-2 Dark I-V measurement 22 Feb 2019

Dark I-V measurement is a powerful technique to analyze the electrical parameters, diagnostic or manufacturing tool of photovoltaic devices without illumination. The dark I-V does not reveal information on short-circuit current, but is more accurate and sensitive than light I-V to give extra parameters such as series resistance, shunt resistance, diode ideality factor, and diode saturation currents [8, 9].

Double-diode model equivalent circuit of a solar cell under dark is shown in Figure 3-9.

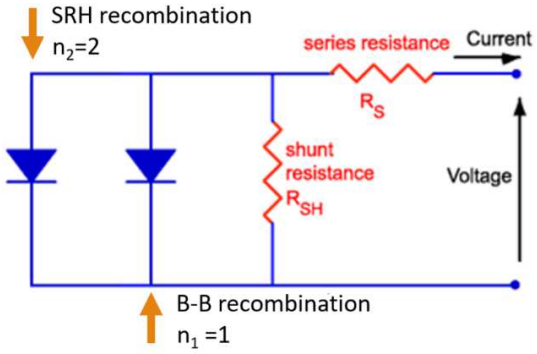

Figure 3-9 Double-diode model equivalent circuit of a solar cell under dark [3].

The dark current equation of the double-diode model under zero illumination is given by,

$$I_{Dark} = I_{01}\left[\exp\left(\frac{q(V + IR_s)}{n_1 kT}\right) - 1\right] + I_{02}\left[\exp\left(\frac{q(V + IR_s)}{n_2 kT}\right) - 1\right] + \frac{V + IR_s}{R_{shunt}} \quad (3.5)$$

The semi-log dark I-V characteristics of a standard silicon photovoltaic cell is shown in Figure 3-10.

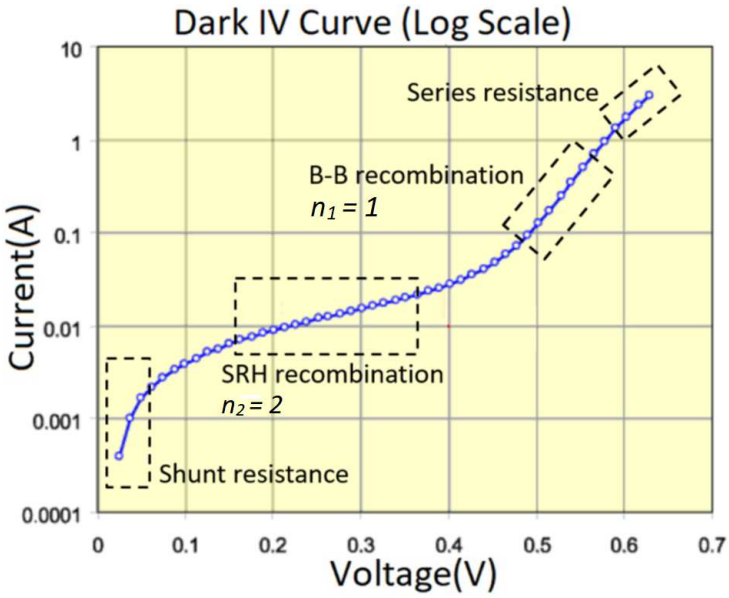

Figure 3-10 Semi-log curve of dark I-V characteristics of a standard silicon photovoltaic cell [8].

Dark current is dominated by shunt resistance at very low voltage range between (0-0.1V). This is normally due to surface leakage loss along the edge of the device, crystal defects, unwanted shunt paths or pinholes in the device.

By increasing the applied voltage further, the dark current equation follows an exponential behavior under two ideality factors. These ideality factors can be derived from the slope of exponential parts of dark IV curve.

Ideality factor for first exponential region under 0.1-0.45V applied voltage is 2. This region is dominated by the recombination in depletion region of photovoltaic device [10]. The factor I_{01} as reverse saturation current is a function of minority carrier lifetime in the depletion region.

$$I_{01} = \frac{qAn_iW}{2\tau} \tag{3.12}$$

Where, q is electron charge, A is device's area, n_i is the intrinsic carrier concentration, W is depletion width, τ is carrier lifetime.

Ideality factor for second exponential region under 0.45-0.6V applied voltage is 1. This region is dominated by the recombination in neutral region of photovoltaic device [10, 11]. The factor I_{02} as reverse saturation current is a function of electron and hole diffusion constants and diffusion lengths.

$$I_{02} = qA\left[\frac{D_n n_p}{L_n} + \frac{D_p p_n}{L_p}\right] \tag{3.13}$$

Where, D_n and D_p are electron and hole diffusion constants respectively. L_n and L_p are electron and hole diffusion lengths respectively. n_p and p_n are the minority carrier concentration.

3-4 Quantum efficiency (QE)

Quantum efficiency is one of the most powerful diagnostic tools in photovoltaic field. QE helps to optimize device thickness, check front and back surface recombination, check bulk recombination, calculate diffusion length, and find out band gap.

External QE (EQE) or QE can be defined the ratio of number collected carriers to the number of incident photons by the solar cell for each wavelength.

$$EQE(\lambda) = \frac{\#\text{ of collected carriers }(\lambda)}{\#\text{ of incident photons }(\lambda)} \tag{3.14}$$

Internal QE (IQE) can be defined the ratio of number collected carriers to the number of absorbed photons by the solar cell for each wavelength.

$$IQE(\lambda) = \frac{\#\text{ of collected carriers }(\lambda)}{\#\text{ of absorbed photons }(\lambda)} \tag{3.15}$$

EQE includes optical loss such as transmission and reflection. On the other hand, IQE includes photons inside the cell which are not transmitted or reflected. Where, R is reflection.

$$IQE(\lambda) = \frac{EQE(\lambda)}{1 - R(\lambda)} \tag{3.16}$$

The schematic quantum efficiency measurement setup is shown in Figure 3-11.

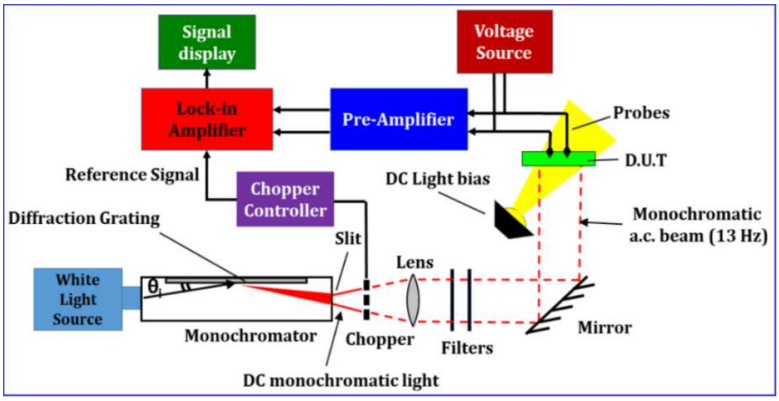

Figure 3-11 Schematic quantum efficiency measurement setup [2].

White light source is generated by a halogen bulb and getting into an optical device called Monochromator that can transmit a selectable wavelength from a wider range of wavelengths available at input by setting appropriate incident angle under diffraction grating mechanism. Later on an optical chopper periodically interrupts the DC light beam and converts it to AC light beam having frequency of 13Hz (See Figure 3-12).

Figure 3-12 Stanford research SR540 optical chopper, Bell Electronics [12].

The output beam from the Monochromator is diverging and light spreads out as it travels. So, a convex lens which is thicker at the middle compare at the edges is used to make the beam parallel. Optical filters to remove harmonics other than the desired wavelength. Order sorting filters are used for order sorting which means they block higher harmonic orders generated by monochromator. The monochromatic light is focused on the device under test (DUT) and

electrical signal amplified by a pre-amplifier and a lock-in amplifier to reduce the noise while is synchronized with the optical chopper. This QE system is also equipped with a voltage and a DC light sources to measure the DUT under applied bias voltage and light.

Quantum efficiency and current density from area and laser can be measured using following equations.

$$QE_{Abs-DUT-Area} = \frac{Signal_{DUT-Area}}{Signal_{Ref-Area}} \times \frac{Area_{Ref}}{Area_{DUT}} \times QE_{Abs-Ref} \quad (3.17)$$

$$J_{Sc-DUT-Area} = \int_{\lambda 0}^{\lambda} q \times \text{Solar Flux} \times \ QE_{Abs-DUT-Area}\, d\lambda \quad (3.18)$$

$$QE_{Abs-DUT-Laser} = QE_{Abs-DUT-Area} \times \frac{Signal_{DUT-Laser}}{Signal_{Ref-Laser}} \times \frac{Signal_{Ref-Laser-632nm}}{Signal_{DUT-Laser-632nm}} \times \frac{Area_{DUT}}{Area_{Ref}} \quad (3.19)$$

$$J_{Sc-DUT-Laser} = \int_{\lambda 0}^{\lambda} q \times \text{Solar Flux} \times \ QE_{Abs-DUT-Laser}\, d\lambda \quad (3.20)$$

Where, $QE_{Abs\text{-}DUT\text{-}Area}$ and $QE_{Abs\text{-}DUT\text{-}Laser}$ are the absolute quantum efficiency of device under test using area and laser respectively. $J_{Sc\text{-}DUT\text{-}Area}$ and $J_{Sc\text{-}DUT\text{-}Laser}$ are the current density of device under test using area and laser respectively.

QE curve for an ideal (brown) and actual (black) crystalline silicon solar cell are shown in Figure 3-13. The quantum efficiency can be presented as a function of both wavelength and energy. QE for a certain wavelength would be unity, if all photons in that wavelength are absorbed and consequently all the generated minority carriers are collected.

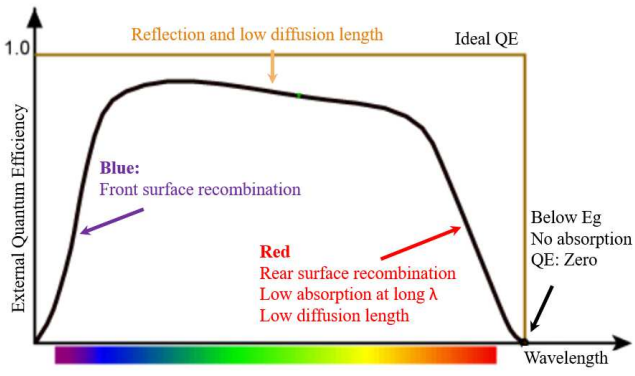

Figure 3-13 External quantum efficiency of a silicon solar cell [13].

QE for blue response (high energy photons) is reduced due to front surface recombination. QE for green response is reduced due to the overall reflection and low diffusion length. QE for red response (low energy photons) is reduced due to back surface recombination, low absorption at long wavelengths and low diffusion lengths, finally QE is zero for incident photons bellow the bandgap.

The internal quantum efficiency under theoretical calculation for a finite solar cell is given by following equation [14].

$$IQE = \frac{\alpha^2 L^2}{\alpha^2 L^2 - 1}\left[1 - \frac{1}{\alpha L}\left(\frac{\frac{SL}{D}\left(\cosh\left(\frac{t}{L}\right) - e^{-\alpha t}\right) + \sinh\left(\frac{t}{L}\right) + \alpha L e^{-\alpha t}}{\frac{SL}{D}\sinh\left(\frac{t}{L}\right) + \cosh\left(\frac{t}{L}\right)}\right)\right] \quad (3.21)$$

Where, α is absorption coefficient, L is minority carrier diffusion length, S is the surface recombination velocity, D is diffusion constant, and t is active layer thickness.

For the crystalline silicon under high enough energy when absorption coefficient is high,

For αt >> 1

$$e^{-\alpha t} \approx 0$$

If t >> L

$$\cosh\left(\frac{t}{L}\right) = \frac{1}{2}\left(e^{\frac{t}{L}} + e^{-\frac{t}{L}}\right) = \frac{1}{2}e^{\frac{t}{L}}$$

$$\sinh\left(\frac{t}{L}\right) = \frac{1}{2}\left(e^{\frac{t}{L}} - e^{-\frac{t}{L}}\right) = \frac{1}{2}e^{\frac{t}{L}}$$

After some simplification

$$IQE = \frac{\alpha^2 L^2}{\alpha^2 L^2 - 1}\left[1 - \frac{1}{\alpha L}\right]$$

IQE equation reduces to

$$IQE = \frac{\alpha L}{1 + \alpha L} \quad (3.22)$$

And diffusion length can be derived from the slop of IQE^{-1} vs. $Alpha^{-1}$.

$$\frac{1}{\mathrm{IQE}} = 1 + \frac{1}{\alpha}\frac{1}{\mathrm{L}} \tag{3.23}$$

3-5 Sub-gap quantum efficiency

Defects distribution is an essential parameter to analyze and evaluate the recombination phenomena in the photovoltaic devices. Sub-gap quantum efficiency (QE) is an interesting technique to measure the mid-gap density of states and tails density of states distribution in a semiconductor (See Figure 3-14 and Figure 3-15). Mid-gap density of states and tails density of states distribution inside the material bandgap follows Gaussian and exponential distribution respectively.

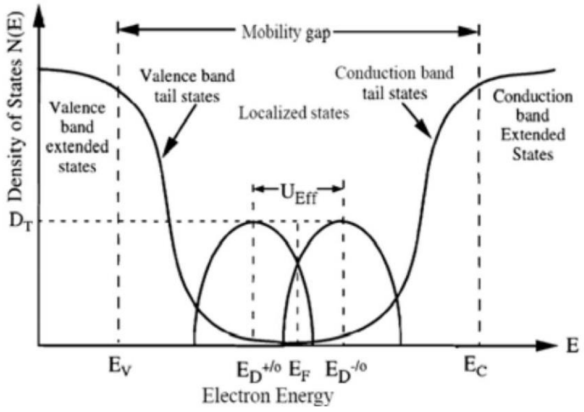

Figure 3-14 Mid-gap density of states (Gaussian) and tails density of states (Exponential) distribution in a semiconductor [15].

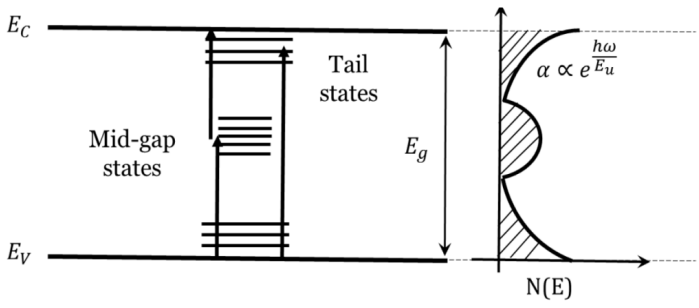

Figure 3-15 Transitions through mid-gap states and tail defect states measured by Sub-gap QE [16].

Absorption coefficient distribution due to tail states exponential decay is given by:

$$\alpha = \alpha_{gap} \times \exp\left[\frac{E_{gap} - E}{E_{Urbach}}\right] \quad (3.24)$$

Where, α_{gap} is the absorption coefficient in the band-edge. E_U is Urbach energy that explains the distribution of tail states inside the forbidden gap of semiconductor material. Higher Urbach energy indicates how defective the material can be. Lower Urbach energy shows better crystalline quality and less tail state in the material.

The absorption coefficient of an a-Si:H film versus photon energy is shown in Figure 3-16. Region (a) is due to transients from valance band to conduction band (band-to-band transients). In region (b) by decreasing the photon energy bellow the bandgap (1.7eV), α drops due to tail states transient. Finally, region (c), deep defects transitions are dominate at very low energy.

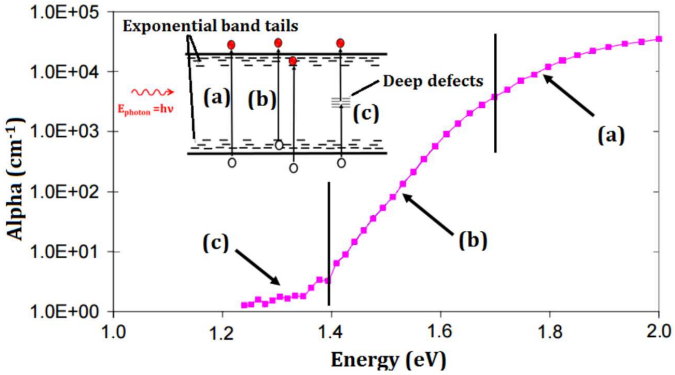

Figure 3-16 Absorption in a-Si:H, (a) band-to-band transition, (b) tail-to-band transition, and (c) deep defects transitions [17].

The Urbach energy and bandgap can be derived using EQE measurement on Solar cell device (Sub-gap). First of all, we need to measure EQE at wavelength close and bellow the bandgap precisely with 5nm step. Then, we should plot Ln (EQE) vs. photon energy. Sub-gap quantum efficiency of a perovskite cell is shown in Figure 3-17.

We know that QE drops below the bandgap. So energy at which QE decreases exponentially gives the bandgap. Urbach energy also is equal to the slop of Ln (EQE) vs. energy in the Band-

Tail state region (Figure 3-17). Urbach energy of amorphous silicon is around 50meV which is much higher than Urbach energy for perovskite that is about 16meV [16].

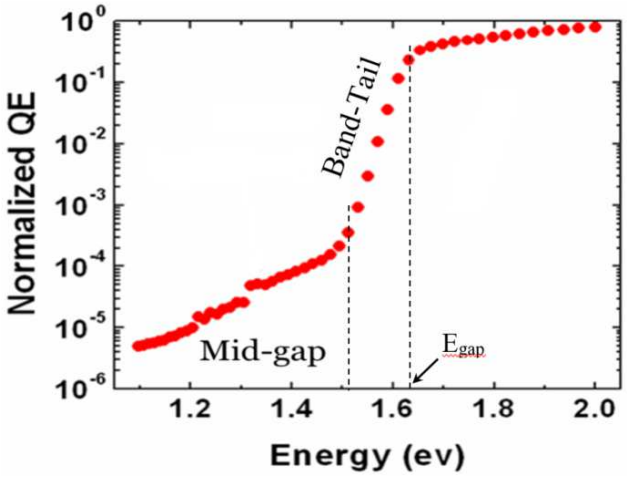

Figure 3-17 Sub-gap QE of perovskite solar cell [16].

3-6 Capacitance vs. voltage (C-V) spectroscopy

Capacitance as a function of voltage (C-V) is standard technique to measure dopant density and depletion width in a PN junction such as solar cell and light emitting diode (LED). Capacitors store electric charges in form of electric filed on two conducting parallel plates which is separated by a dielectric or insulating layer. PN junction in reverse biased also store charges inside the depletion region (See Figure 3-18).

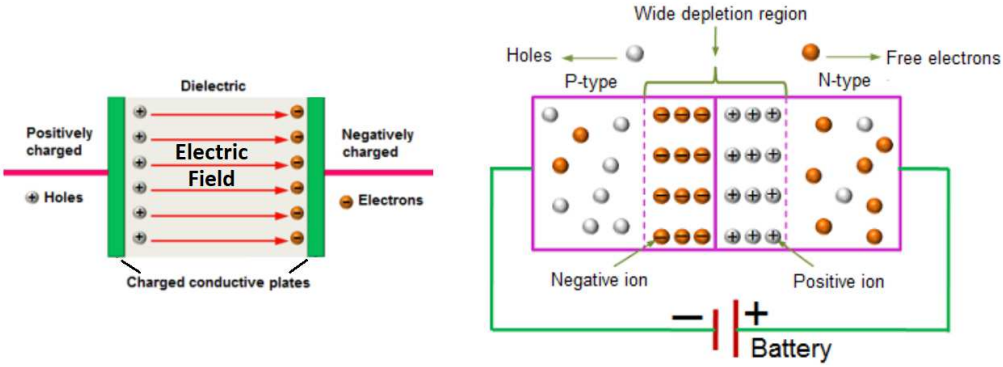

Figure 3-18 Parallel plate and diode junction capacitance [18].

A PN junction without bias, under reversed-biased and corresponding energy band diagrams are shown in Figure 3-19.

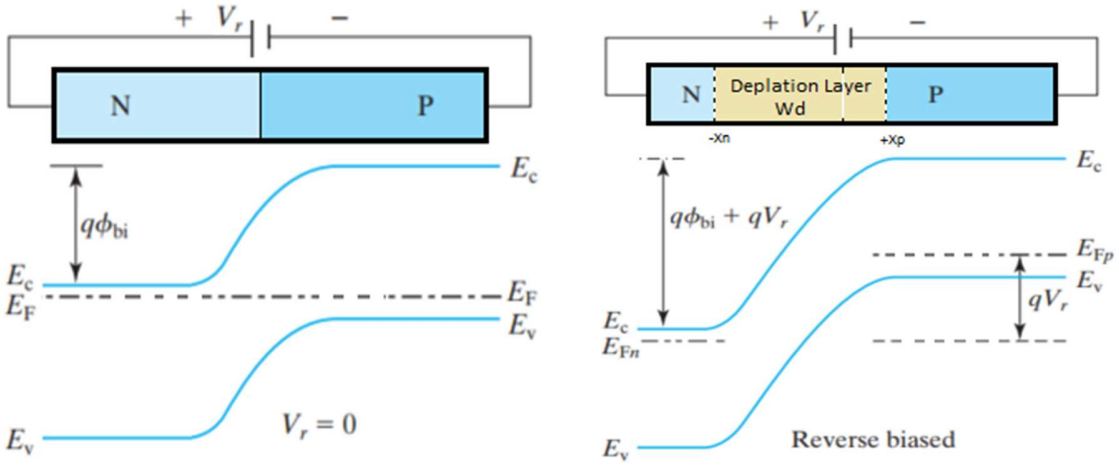

Figure 3-19 PN junction energy band diagram without bias (Left), PN junction energy band diagram with reverse bias (Right) [19].

Under reverse bias, depletion region width and potential barrier increase (from $q\Phi_{bi}$ to $q(\Phi_{bi}+V_r)$. In the same way, holes have to go from N side to P side and electrons have to go from P side to N side. Since there are few holes and electrons (minority carriers) in N side and P side respectively, then current is very small. As it shown in Figure 3-20, the PN junction can be considered as a parallel-plate capacitor since N and P layers act as two conductors and depletion layer acts as an insulator.

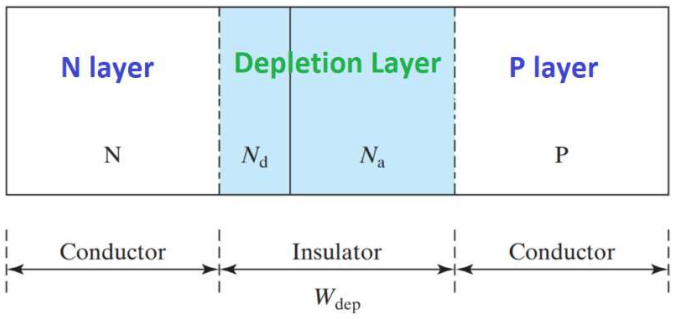

Figure 3-20 PN junction as a parallel-plate capacitor [19].

Depletion width (W_{dep}) and depletion capacitor (C_{dep}) for a PN junction are given by:

$$W_{dep} = \sqrt{\frac{2\epsilon(V - V_{bi})}{qN_D}} \tag{3.25}$$

$$C_{dep} = \frac{\epsilon A}{W_d} = A\sqrt{\frac{q\epsilon N_d}{2(V - V_{bi})}} \tag{3.26}$$

Here, ϵ is dielectric constant, V is applied voltage across the junction, V_{bi} is built-in voltage, N_d is dopant density of lightly doped layer, and A is device area. If we plot $1/C^2$ vs. applied voltage, the dopant density can be find from the slop. Built-in voltage is the intercept of straight line with horizontal axes.

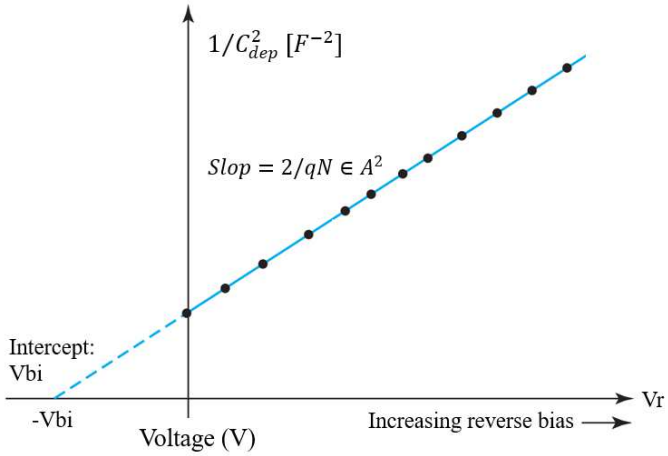

Figure 3-21 the standard capacitance vs. voltage plot of a PN junction [19].

3-7 Capacitance-Frequency vs Temperature (CFT)

The distribution of electronic defects inside a semiconductor bandgap can be investigated using CFT technique. In this technique, the device capacitance is measured under a zero bias by varying the frequency of the AC signal for different temperature. This is a well-known

technique to study the density of states which play an important role in recombination phenomena of photo-generated minority carriers.

The emission rate of an electron form a trap state with energy level E_T bellow the conduction band can be expressed by [16, 20]:

$$e_n = N_c v_{th} \sigma_n \exp\left(-\frac{E_A}{kT}\right) \text{ where } E_A = E_C - E_T$$

Where, e_n is emission rate, N_c is the effective density of states, v_{th} is thermal velocity, σ_n is the capture cross section of trap. k is the Boltzman constant, and T is temperature in Kelvin E_A, E_C, E_T are activation, conduction band, and trap energies respectively.

The schematic diagram of traps with different energy levels is shown in Figure 3-22.

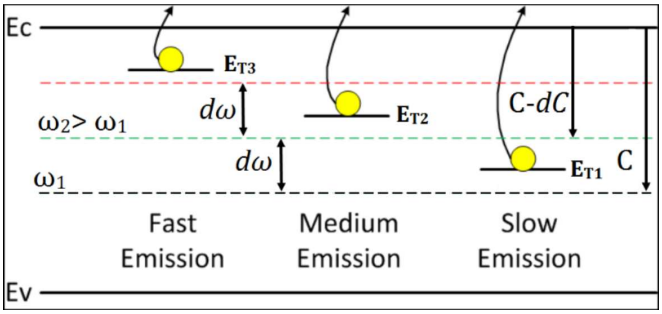

Figure 3-22 Schematic diagram of shallow, medium, and deep traps inside a semiconductor material [2].

The shallow traps have fast emission rate, so they can response to both low and high frequency. The deeper traps have slower emission rate, so they can't response to high frequency, they response only to lower frequency. Under lower frequency both shallow and deeper traps contribute to capacitance spectroscopy, but under higher frequency only shallow traps contribute to capacitance measurement. So by increasing the frequency the value of capacitance decreases.

The temperature-dependence of the effective density of states and thermal velocity are given by:

$$N_C \propto T^{\frac{3}{2}} \quad \text{and} \quad v_{th} \propto T^{\frac{1}{2}}$$

So, attempt to scape frequency (ATSF) can be explained by

$$\text{ATSF} = v_0 = N_c v_{th} \sigma_n = \xi \times T^2$$

By re-writing the emission rate of an electron form a trap state

$$e_n = \xi \times T^2 \exp\left(-\frac{E_A}{kT}\right)$$

$$\frac{e_n}{T^2} = \xi \exp\left(-\frac{E_A}{kT}\right)$$

Attempt to scape frequency and activation energy can be derived from the intercept and slop of the Arrhenius plot of $\text{Ln}(f_{peak})$ vs (1/kT) respectively.

$$\ln\left(\frac{e_n}{T^2}\right) = \ln\left(\frac{f_{peak}}{T^2}\right) = \ln(\xi) - \frac{1}{kT} E_A$$

The f_{peak} can be derived by plotting –f dC/df vs frequency. So, the peaks are correspond to ATSF at different temperatures. Finally, the density of state (DOS) can be find by derivation of capacitance vs frequency [21, 22].

$$\text{DOS} = N_T(E_\omega) = -\frac{V_{bi}}{qW_d}\frac{dC}{d\omega}\frac{\omega}{kT}$$

Where, V_{bi} is the built-in voltage, C is capacitance, ω is angular frequency ($\omega=2\pi f$), W_d is the depletion width. DOS has to be plotted vs E_ω as a "probing depth" that can be calculated from the demarcation energy.

$$E_\omega = kT\ln\left(\frac{\omega}{\omega_0}\right) \qquad \text{where} \qquad \omega_0 = 2\pi\nu_0$$

Where ω_0 is angular ATSF and ν_0 is ATSF.

The typical capacitance vs frequency at room temperature and DOS vs energy for a perovskite cell are shown Figure 3-23.

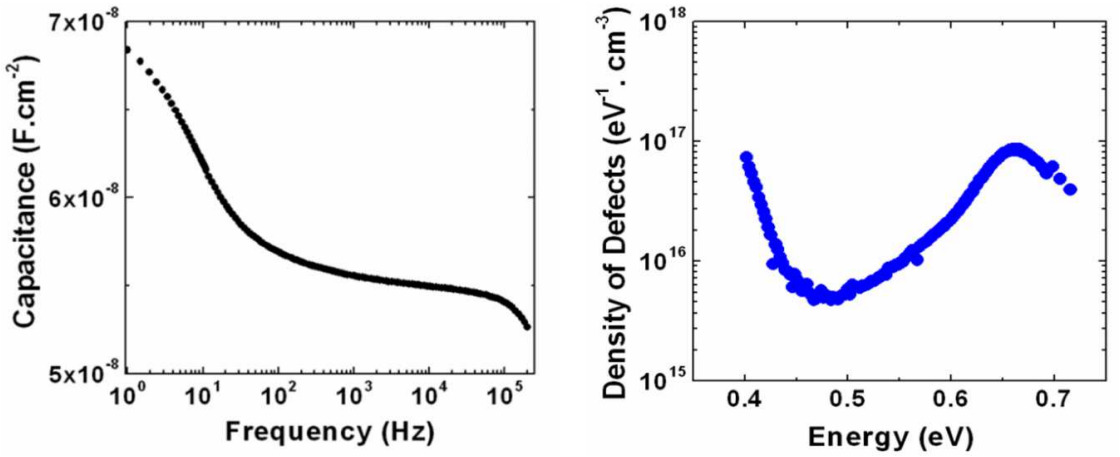

Figure 3-23 Capacitance vs frequency and DOS vs energy for a perovskite solar cell [15].

3-8 Photoconductivity

Photoconductivity is an optical and electrical phenomenon in which a material becomes more electrically conductive due to the absorption of incident photons or electromagnetic radiation. The mobility-lifetime product ($\mu\tau$) as one of the important transport parameters in photo-conductor or solar cell applications can be measured using photoconductivity. This product is related to the transport property of the material and indicates how well a material will be suitable as a solar cell. Large carrier mobility indicates how fast the optically generated carriers travel towards the terminals and large lifetime shows low recombination probability of the carriers. So, larger of the $\mu\tau$ product, represents that larger percentage of light generated

carriers will be collected before recombination. So, larger μτ product is required for an effective photovoltaic device. Device structure for photoconductivity experiment is shown in Figure 3-24. Current vs. voltage characteristic is measured through two aluminum, silver, or gold bars under dark and light illumination (AM1.5) inside a dark box.

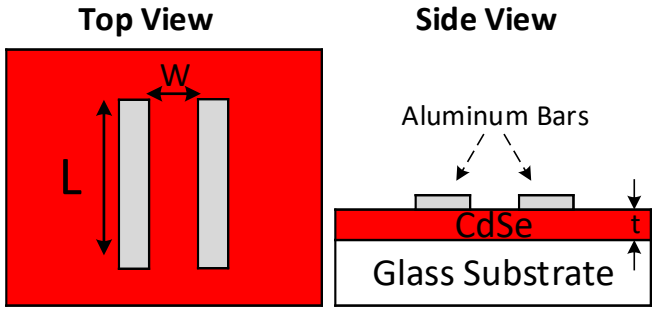

Figure 3-24 Device structure to measure mobility-lifetime product using photoconductivity.

Conductivity and resistivity of thin film is calculated by

$$\rho = R \times \frac{L.\,t}{W} \tag{3.27}$$

$$\sigma = \frac{1}{\rho} \tag{3.28}$$

Where, ρ, R, L, t, W, and σ are resistivity, resistant, length of metal bars, film's thickness, distance between two parallel bars and conductivity respectively.

A reference silicon solar cell can be used to measure number of incident photons (N_0).

$$N_0 = J_{sc}/(q.\,QE) \tag{3.29}$$

Where, J_{sc}, q, and QE are current density, electron charge, and quantum efficiency of reference silicon cell respectively.

Number of absorbed photos (N_{abs}) and generation rate (G) are given by

$$N_{abs} = N_0\,(1-R)(1-\exp(-\alpha t)) \tag{3.30}$$

$$G = N_{abs}/t \tag{3.31}$$

Where, R, α, and t are reflection, absorption coefficient, and thickness respectively.

Finally, photoconductivity and mobility-lifetime product can be expressed by

$$\Delta\sigma = \sigma_{\text{Light}} - \sigma_{\text{Dark}} \tag{3.32}$$

$$\mu\tau = \Delta\sigma/qG \tag{3.33}$$

Where, σ_{Light}, σ_{Dark}, and $\Delta\sigma$ are light conductivity, dark conductivity, and photoconductivity respectively.

3-9 Space charge limited current (SCLC)

Space Charge Limited Current (SCLC) [23] is an interesting method to measure mobility and carrier concentration in semiconductor materials. In this technique, there are two Ohmic contacts on the both sides of thin film to measure current vs. voltage characteristic (see Figure 3-25).

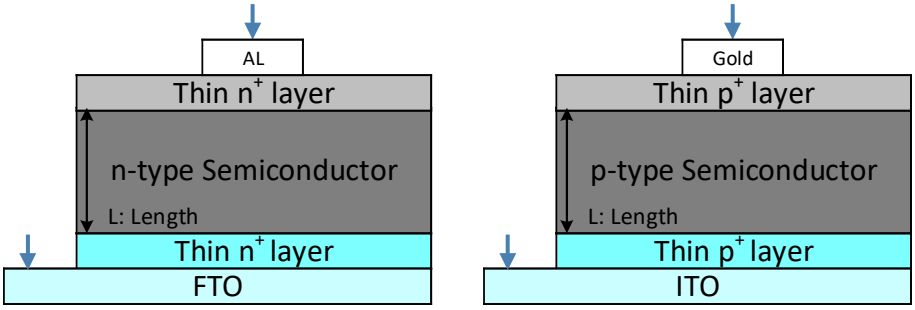

Figure 3-25 Device structure to measure mobility of a semiconductor thin film using SCLC.

Charge carriers are injected into the sample through the Ohmic contacts. At low voltage region, under low electric field the current vs voltage follows an Ohmic law. In Ohmic region, the current is mainly driven by the mobile charge carriers which are presented intrinsically in the material.

$$J = N_0 e\mu \frac{V}{L} \tag{3.34}$$

On the other hand, at high voltage region under high electric field, the current is no longer Ohmic but follows quadratic relation $J \sim V^2$.

$$J = \frac{9}{8} \in \mu \frac{1}{L^3} V^2 \tag{3.35}$$

Where, J is current density, N_0 is thermal carrier concentration, $\in$ is permittivity of material, μ is mobility, L is film thickness, and V is applied voltage.

In SCLC region, the current is not related to charge carrier density, but it only depends on the mobility of carrier. So, the mobility can be calculated from the slop of J vs. V^2.

Current - voltage characteristic of a 50nm CuPc on 10um spacing Au electrode for both Ohmic and SCLC regions is presented in Figure 3-26.

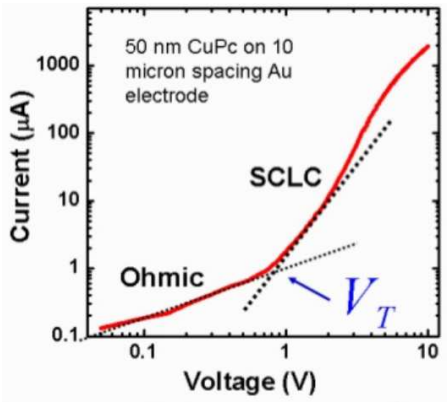

Figure 3-26 Macroscopic view of charge transport for Ohmic and SCLC conduction [24].

Carrier concentration also can be measured in SCLC technique using

$$n = \in \frac{1}{q} V_{SCLC} \frac{1}{L^2} \tag{3.36}$$

Where, n is carrier concentration, q is electron charge, V_{SCLC} is voltage at space charge limited region.

3-10 Scanning electron microscope (SEM)

Scanning electron microscope is an electron microscope that utilizes high energy focused electron beam (~0.1nm) to generate high magnified images and variety of signals. These signals provide several useful information regarding surface morphology, material composition, crystalline structure and orientation. SEM uses electrons to create very high

magnification (100Kx) images compare to optical microscope that uses photons to create limited magnification (1.5Kx) images. Because the wavelength of electrons (0.01nm) is much lower than the wavelength of photons (400-700nm) with much higher depth of filed (DOF) for electrons compare to photons. The schematic diagram of a standard SEM including the electron optical column and the image formation process is shown in Figure 3-27. The electron optical column includes electron gun, condenser aperture and lens, scanning coils, objective lens and aperture, detectors to collect secondary electrons, backscattered electrons, and X-ray photons, scanning circuit, and cathode ray tube (CRT) display.

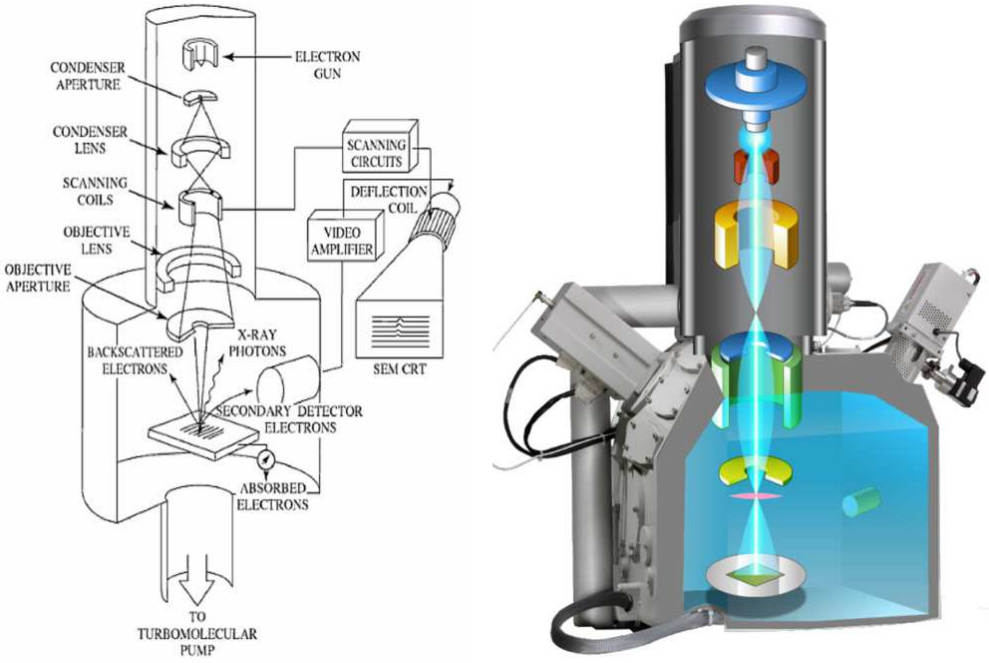

Figure 3-27 Schematic diagram of a Scan Electron Microscope [25, 26].

The electron gun produces intense and high energy electrons beam. Three basic electron gun types are tungsten thermionic filament, LaB6 thermionic filament, and tungsten filed emission filament. Electromagnetic lenses de-magnify the electron beam to make beam sharp. Condenser lens controls the number of electrons corresponds to the size of objective aperture,

and the objective lens centralizes electrons on the specimen corresponds to the working distance. The diameter of aperture controls the number of electrons passing through. Scan coil scans (raster) the beam across the sample. Finally, detectors (Like secondary electrons, backscattered electrons, x-rays) collect the signals to create SEM images on CRT display or determine related information regarding the sample after appropriate amplification and processing. In this project, we measured SEM images to study the grain growth on the top surface and cross-section of CdSe thin film.

3-11 Energy dispersive x-ray spectroscopy (EDS)

EDS is a qualitative and quantitative X-ray technique to analyze the chemical composition and characterization of materials. A graphical view of EDS principal is shown in Figure 3-28. To produce X-ray characteristic signal, a primary high energy electron (E_0, e) hits the inner line (K-line) atom of a specimen to ionize it and generate an electron-hole pair. Secondary electron kicks out and a higher line (L-line) electron drops into vacant K-line to fill the hole. The characteristic X-ray signal is emitted due to energy difference between L-line and K-line. The X-ray lines are called based on inner and higher lines which the initial vacancy occurs and electron drops into that vacancy respectively.

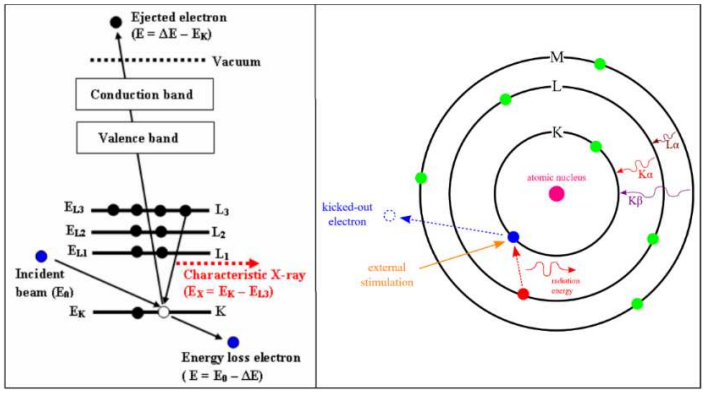

Figure 3-28 Energy dispersive X-ray spectroscopy (EDS) principal [27, 28].

A schematic diagram of X-ray detector is shown in Figure 3-29. Collimator assembly acts as limiting aperture which allows X-ray pass into the detector. Electron trap includes a pair of permanent magnet to prevent passing through any electrons would cause background artifacts. Window is a transparent barrier to maintain vacuum while passing X-ray signal into detector. Incident X-ray signal inside detector's semiconductor crystal creates electron-hole pairs based on ionization effect. Generated electron-hole pairs are collected under high applied voltage to produce a charge signal. Filed effect transistor (FET) amplifies the charges that are created previously by the crystal. These charges build up and restore on a feedback capacitor. Detector signal to noise ratio has to be improved by reducing the electronic noise. Electronic noise can be reduced by cooling down the crystal and FET using liquid nitrogen.

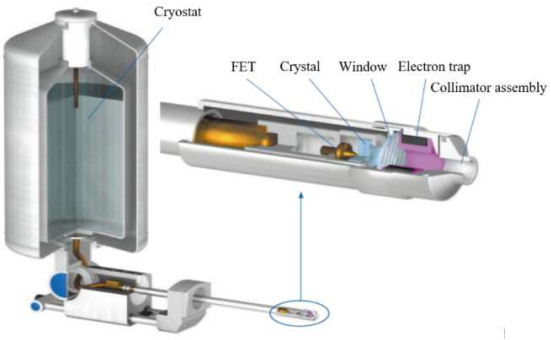

Figure 3-29 X-ray detector [27].

When acceleration voltage goes up, electron gets higher energy to penetrate more in depth. So interaction volume increases. Resolution as the ability to resolve between two closely space points increases when acceleration voltage goes up.

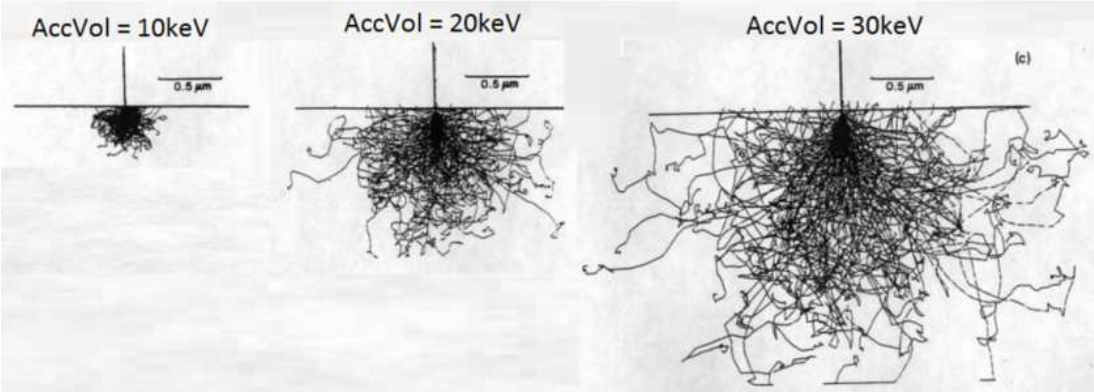

Figure 3-30 Monte Carlo calculations of the interaction volume in iron for various acceleration voltage [29]

In this work, CdSe thin film composition (Atomic % of Se/Cd) was studied using energy dispersive X-ray spectroscopy technique.

3-12 References

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CHAPTER 4. CADMIUM SELENIDE THIN FILMS GROWTH, IMPROVEMENT AND CHARACTERIZATION FOR SOLAR CELL APPLICATION

4-1 Introduction

As it mentioned before, photovoltaic technology is an important technology to convert sunlight to useable electrical power with significant potential for reducing global warming. Silicon in both forms of crystalline and amorphous is the most well-known material in photovoltaic industry. The best research cell efficiency chart is shown in Figure 4-1.

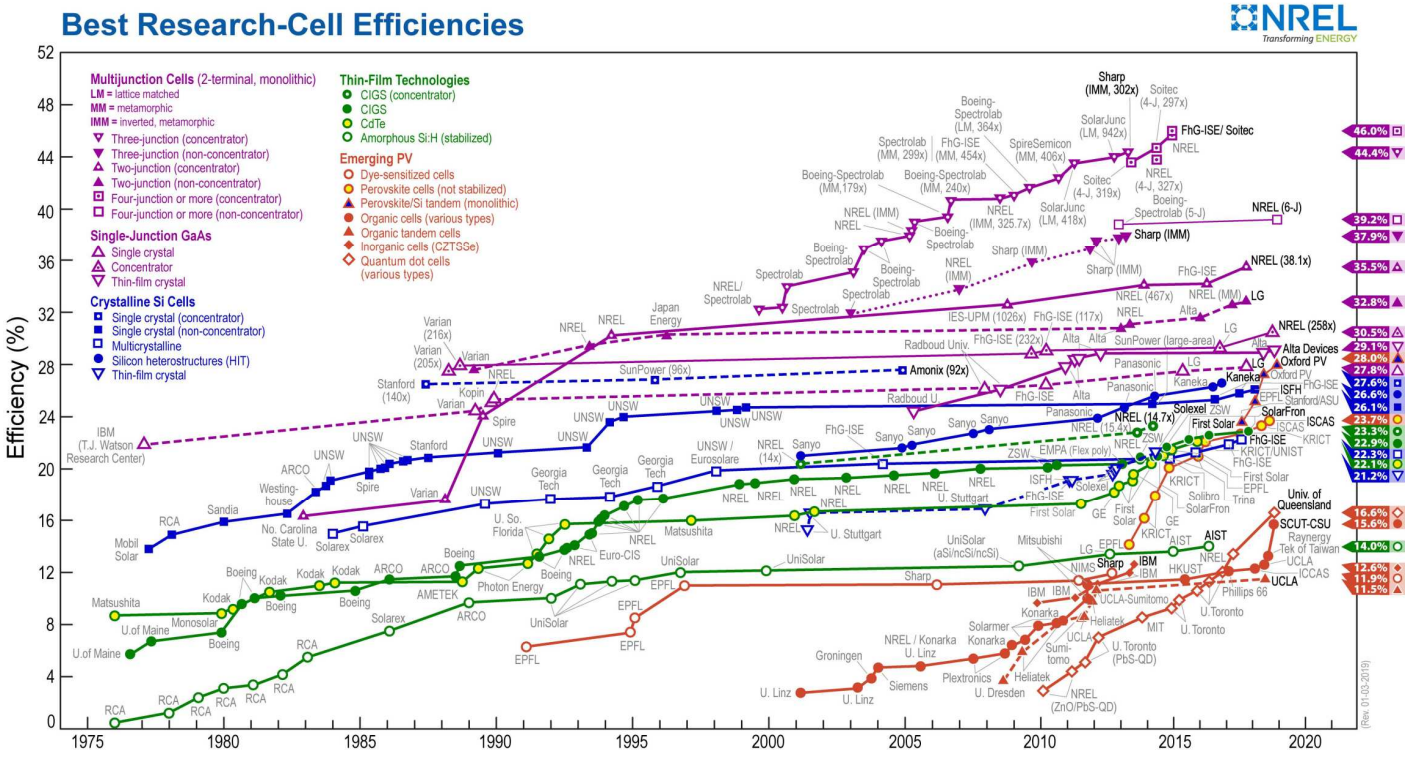


Figure 4-1 PV research cell record efficiency chart, NREL, 2018 [1].

The costs of the PV solar energy system currently are dominated by several factors like system, structural, field wiring, chemical encapsulation materials, and glass costs. Although the cost of silicon cells has reduced remarkably during the past decade, we still need to discover new materials and invent novel device designs to make solar energy more economical. In order to

make PV technology cost-competitive with other conventional sources of energy and significantly reduce the total costs of PV technology, the conversion efficiency needs to be increased, due to proportional relationship between the system cost reductions with an increase in efficiency. One of the interesting way to achieve high efficiency cell is to use a tandem junction solar cell, comprising two materials, one with higher bandgap material as top cell and another with lower bandgap material as bottom cell.

The contour plot for two junction series connected tandem solar cell design is shown in Figure 4-2. The top cell (higher bandgap) absorbs high energy photons and the bottom cell absorbs low energy photons. Theoretically the maximum efficiency for a two junction tandem (series connected) could be around 47% under a top cell with bandgap of 1.63eV and bottom cell with bandgap of 0.96eV [2].

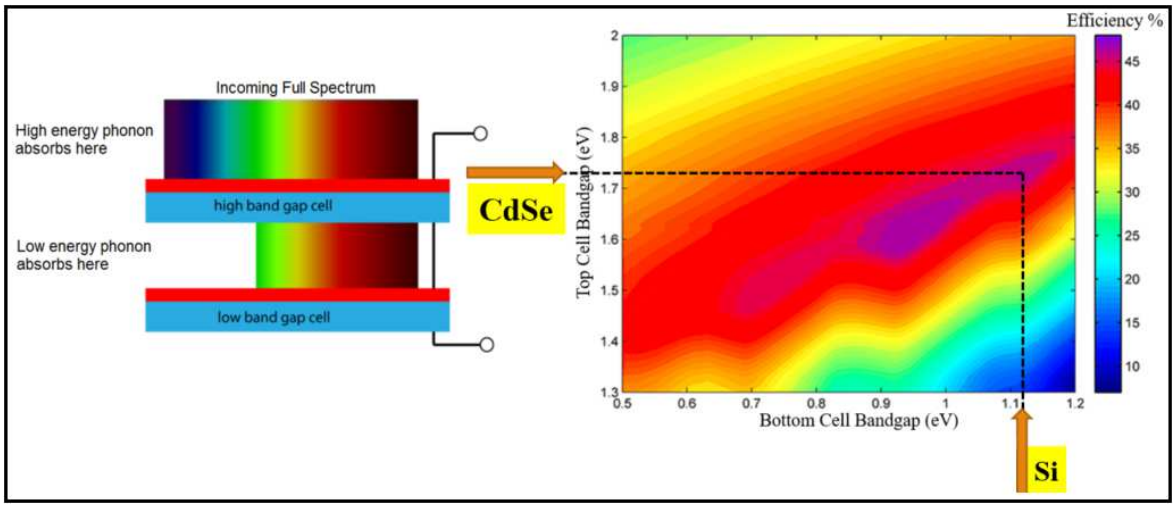


Figure 4-2 The maximum efficiency for a two junction tandem under the AM1.5G spectrum [2].

Theoretical calculations indicate that it is possible to attain a thermodynamic efficiency more than 40% for a tandem cell of cadmium selenide with bandgap of 1.72eV [3-5] as top cell and crystalline silicon with bandgap of 1.125eV as bottom cell [6].

Two types of tandem cell configuration as unconstrained stack and constrained are shown in Figure 4-3. Unconstrained stack is designed to operate at its maximum power point under separate circuit connection for each cell. But, constrained stack is designed to have only two electrodes for the whole stack under series circuit connection. Mismatch in the output current for each cell is one of the main concern in constrained stack design.

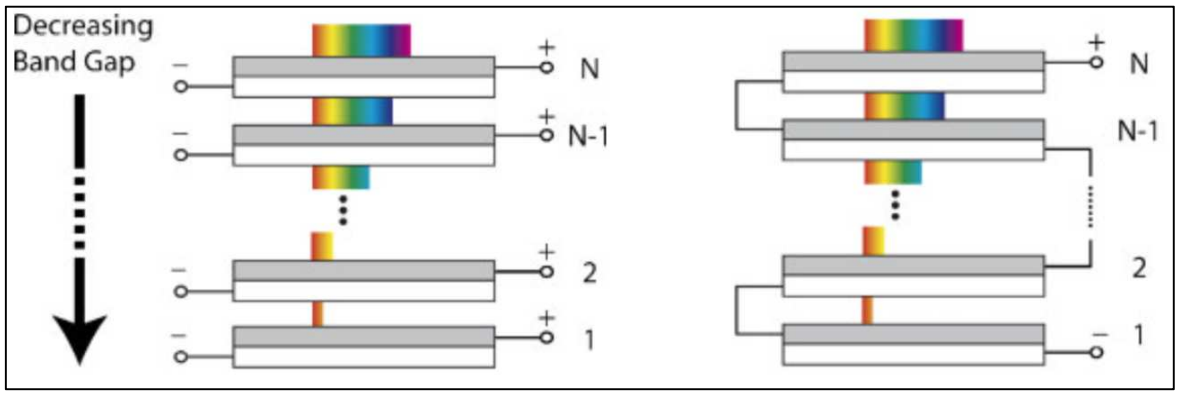


Figure 4-3 Tandem solar cell stack, Unconstrained (Left), Constrained (Right) [7].

Figure 4-4 shows the power conversion efficiency of the stack can be significantly increased by increasing the number of bandgaps. But in reality there aren't semiconductor materials available with any arbitrary bandgap.

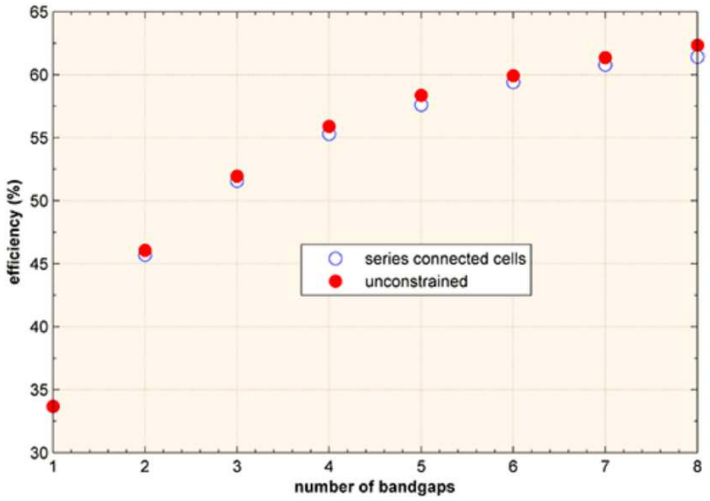


Figure 4-4 Efficiency of a an ideal stack of solar cells as a function of the number of bandgaps [2, 7].

4-2 Cadmium selenide (CdSe)

CdSe is an inorganic binary-compound highly photosensitive semiconductor. Stoichiometry is easier to achieve in CdSe compare to ternary or quaternary compound. CdSe is a n-type direct band gap material that is classified as a II-VI semiconductor with high absorption coefficient in the visible region of solar spectrum [8, 9]. CdSe is not water soluble and does not thermally decompose, unlike Pb-halide perovskites [10]. CdSe is mainly available for research purposes in from of chunk or powder (Figure 4-5).

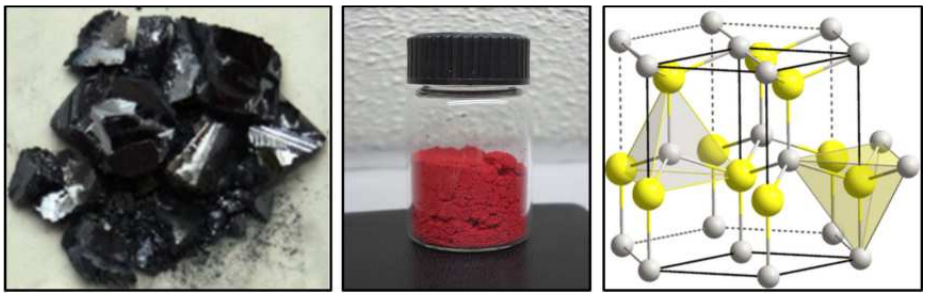


Figure 4-5 CdSe chunk (left), power (middle), and wurtzite crystalline strucutre (right) [11].

Three different crystalline structures are exist for CdSe such as wurtzite (hexagonal), sphalerite (cubic), and rock-salt (cubic). The wurtzite is the most stable structure for CdSe compare to two others. The sphalerite structure for CdSe isn't stable and convert to the wurtzite structure under moderate temperature. Finally, the rock-salt CdSe structure is just found under high pressure condition [11, 12].

Two main different methods for production of bulk crystalline cadmium selenide have been reported like the High-Pressure Vertical Bridgman or High-Pressure Vertical Zone Melting [11, 13]. D .Bonnet et al, also were reported their own method of high purity CdSe (6N) production in laboratory [4]. Cadmium and Selenium elements in stoichiometric proportion were mixed and sealed in a quartz ampoule under vacuum. High purity CdSe performs under

high temperature reaction inside a furnace (T>1000°C). One side of the ampoule was placed at lower temperature around 700°C in order to avoid extreme pressure [4].

4-3 Deposition techniques of CdSe

Cadmium selenide thin films can be deposited using the several techniques such as thermal evaporation (TE) [4], close space sublimation (CSS) [14, 15], sputtering [16] and electron e-beam deposition, and. These techniques are widely used for mass-production of cadmium telluride (CdTe) and copper indium gallium diselenide (CIGS) solar cells in industry.

4-3-1 Close space vapor transport (CSVT)

One of the common physical vapor deposition (PVD) method for deposition of CdSe thin films is close space vapor transport (CSVT) [13] or close space sublimation (CSS) [14, 15]. In CSS, the source is located in very short distance from substrate (1-2mm or less) and source materials evaporate under 600°C to 800°C heat and condense on substrate in both vacuum and atmospheric pressure. Deposition rate under CSS is very high, so 1-10um cadmium telluride thin film can be deposited within 10 minutes [17]. The schematic diagram for CSVT design is shown in Figure 4-6. The reactor consists of two pyrolytic graphite heaters were placed in a quartz tube.

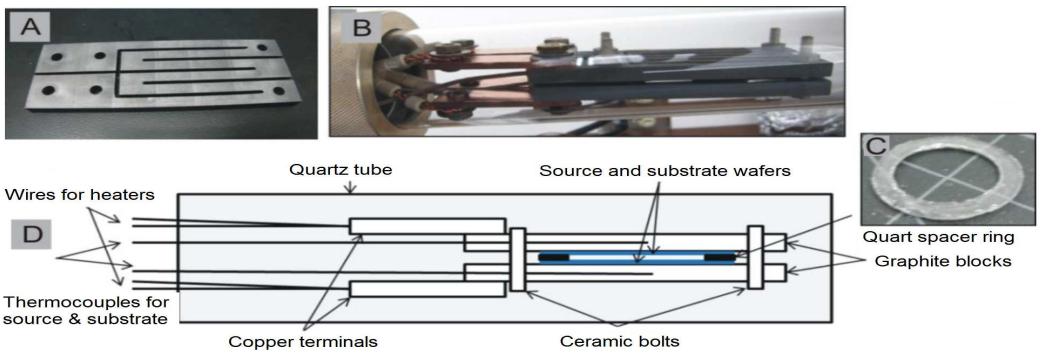


Figure 4-6 Schematic diagram of CSVT system [14].

The close view schematic diagram for CSS design is shown in Figure 4-7. The source and substrate are separated by 1mm distance inside a fused silica tube. Two lamp heaters provide appropriate temperatures under infrared radiation, where two mounted thermocouples monitor the temperatures. CSS process mostly performs at pressure between 1 to 30Torr, substrate temperature between 500 to 600°C and source temperature in the range of 700 to 800°C [17].

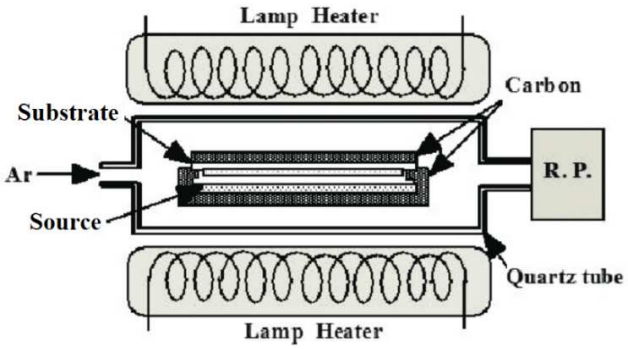


Figure 4-7 Schematic diagram of a CSS system [17].

4-3-2 Thermal evaporation (TE)

Thermal evaporation (TE) is a common PVD technique of creating CdSe thin films [4]. Cadmium selenide research project at Iowa State University (ISU), Microelectronic Research Center (MRC) has been done mainly using thermal evaporation. So, I am going to take a short look at the implementation of this system.

The schematic diagram for a standard TE system is shown in Figure 4-8. With TE, materials will evaporate form a source under enough heat (300-800°C) in high vacuum ($\approx 10^{-6}$ Torr) and finally the evaporated materials condense on a substrate in order to create thin film. The source can be heated either by an Ohmic resistance boat or LUXEL furnace depends of the materials (see Figure 4-9). All boats and crucibles are made from refractory metals like tungsten, molybdenum, tantalum, and alumina since they don't contaminate thin films due to their high melting points. The deposition parameters such as rate and thickness are controlled

using several factors like applied current through the boat and crystal thickness monitor. A crystal thickness monitor measures deposition rate and thickness using a quartz crystal microbalance (QCM). The amount of material that is deposited on the crystal, changes the resonant frequency of crystal. So, the thickness can be calculated by converting resonant frequency to electrical signal and density of material.

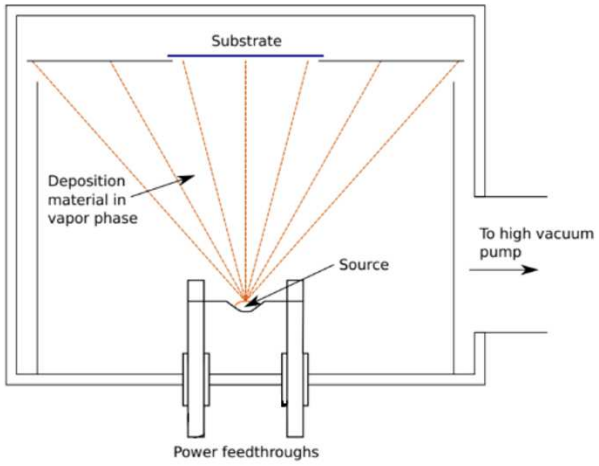


Figure 4-8 Schematic diagram of a thermal evaporation system [18].

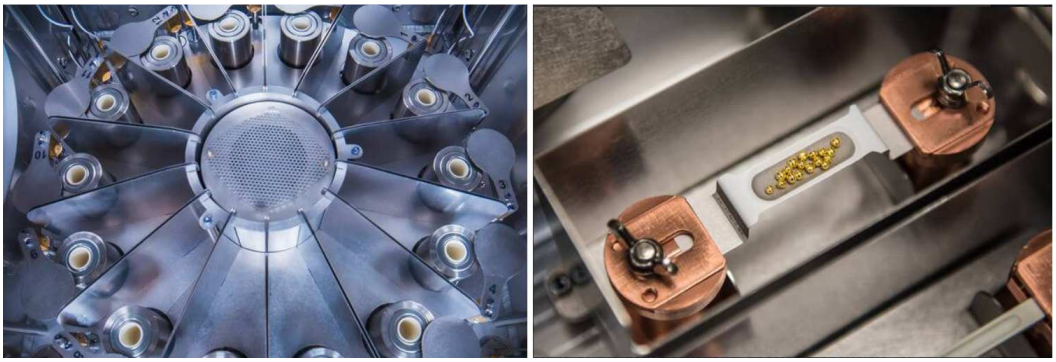


Figure 4-9 LUXEL furnaces (left) and an ohmic resistance boat (right) [19].

As it is shown in Figure 4-10, under thermal evaporation, evaporated source travels in a straight direction. In this circumstance, the deposition rate for any particular distance from a point source is given by following equation

$$\rho = \frac{E}{r^2} \tag{4.1}$$

Where, ρ is the deposition rate at distance r from the source, E is the evaporation rate at the source, and r is the distance from source to deposition surface (substrate).

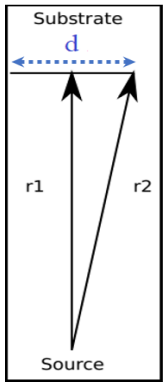


Figure 4-10 geometry of an evaporation (right) [18].

Gk Since the deposition rate across a substrate depends on distance (r) from the source, uniformity as a critical parameter can be achieved by considering distance (r) large enough compare to size of substrate (d).

For example, the deposition uniformity for TE at ISU-MRC for r1= 30cm, d= 2.5cm is about 99.98%.

$$\frac{\rho_2}{\rho_1} = \left(\frac{r_2}{r_1}\right)^2 = \frac{(30cm)^2}{(30cm)^2 + (0.5 \times 2.5cm)^2} = 0.9998 \tag{4.2}$$

4-3-3 E6 Thermal Evaporation system at Iowa State University (ISU), Microelectronic Research Center (MRC)

A new thermal evaporation system (E6-TE) was made for this project to make uniform, high quality, and reproducible CdSe films. E6-TE consists of a stainless steel evaporation chamber, rotary and turbo vacuum pumps, substrate heater, two Luxel RADAK furnaces with thermocouples, crystal thickness monitor, and two HP power supplies. System pumps down to 10^{-7} Torr and substrate heater can be heated up to substrate up to 500°C. Deposition rate and

film thickness can be controlled by adjusting current through the furnaces and thickness monitor. System is equipped with two shutters for both source and substrate to start and stop deposition process.

Figure 4-11 Photograph of the E6 Thermal Evaporation system at ISU-MRC taken at March of 2019.

4-4 Experiments to improve CdSe

In this section, we will explain how to improve CdSe thin films quality using several techniques such as Cadmium Chloride ($CdCl_2$) treatment, Post-deposition selenization, and CdSe deposition with selenium (Se) flux.

4-4-1 Cadmium Chloride (CdCl2) treatment

Cadmium chloride ($CdCl_2$) treatment is a vital process to obtain recrystallization, grain growth and passivation of grain boundaries. The mechanism may involve the growth of grains at the present of chlorine or halogens which acts as fluxing agent. Thereby the atomic diffusion barriers decompose at grain boundaries and promote the crystalline quality [20]. The treatment

process reduces the density of mid-gap states inside the bandgap, also decreases the density of defects in the junction region which helps to passivate the grain boundaries and prevents from recombination [21].

The $CdCl_2$ treatment can perform using solution (drop, dipping, and spin coating) or evaporation methods, followed by a thermal annealing at high temperature under nitrogen atmosphere inside a quartz tube. Annealing in dry air resulted in the film oxidizing into CdO. In this project, we developed $CdCl_2$ process by spin coating of $CdCl_2$ solution onto the CdSe films surface, then thermal annealing under nitrogen atmosphere for various temperature and time. Finally, samples were rinsed in deionized water to remove extra $CdCl_2$ residual from the surface. The schematic diagram of the $CdCl_2$ heat treatment quartz tube furnace is shown in Figure 4-12.

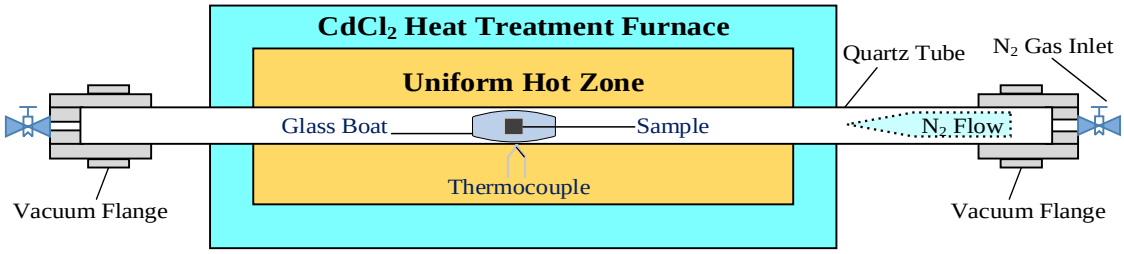


Figure 4-12 Schematic diagram of $CdCl_2$ heat treatment quartz tube furnace.

4-4-2 Post-deposition selenization

As we explained before, CdSe is a binary-compound semiconductor. But there is a chance to get non-stoichiometric CdSe film, especially at high substrate temperature deposition due to difference vapor pressure of Selenium compare to Cadmium. Also selenium mostly evaporates during $CdCl_2$ treatment especially at high temperature annealing. So, post-deposition selenization plays an important role to increase selenium to cadmium ratio and makes it stoichiometric.

The schematic diagram of the two-zone selenization quart tube furnace is shown in Figure 4-13. This system includes two uniform zones. Selenium pellets evaporate from uniform hot zone #1 at 320-330ºC and evaporated selenium travels under nitrogen gas flow and finally is deposited on sample surface which is located at uniform hot zone #2.

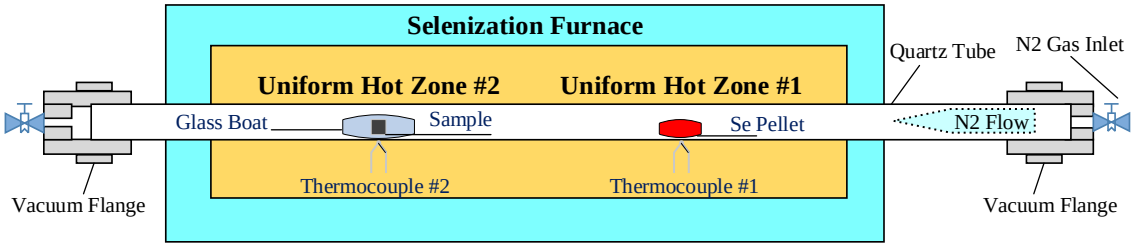


Figure 4-13 Schematic diagram of two-zone selenization furnace, Zone #1: Se evaporation at ~330ºC and Zone #2: Sample at 330ºC [22].

4-4-3 CdSe deposition with selenium (Se) flux

Another technique to increase the ratio of selenium to cadmium is CdSe deposition under Selenium flux. This process is very similar to co-evaporation technique which different elements can be evaporated simultaneously to create semiconductor compound. As we explained before, E6-TE is equipped with two Luxel RADAK furnaces with thermocouples so we are able to exactly adjust and control deposition rates for both CdSe and Se separately. A photo of E6-TE including two furnaces is shown in Figure 4-14

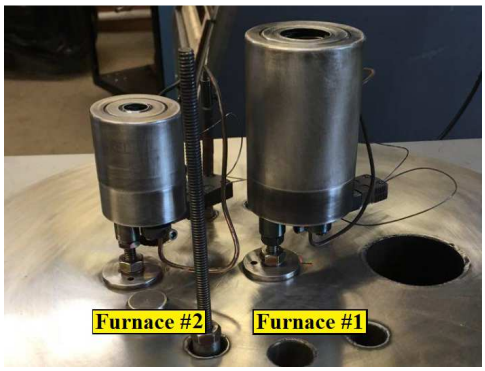


Figure 4-14 E6-TE with two LUXEL furnaces to evaporate CdSe with Se flux.

4-5 CdSe thin films preparation and characterization

In this section, we present the optical, electrical, and morphological properties of CdSe thin films were prepared using thermal evaporation method on various substrates, including glass, fluorinated tin oxide (FTO), indium thin oxide (ITO) [23, 24].

4-5-1 Optical properties

The optical properties of CdSe thin films were measured using Cary 5000 UV-Vis-NIR spectrophotometer for 400–2500nm range of wavelength. 1um CdSe film was deposited on micro glass at 350ºC substrate temperature. Transmission, reflection, and absorption spectrums show the CdSe is about 80% transparent from 720nm to 2500nm while significant absorbance from 400nm to 720nm (Figure 4-15) . The absorption coefficient (α) vs. energy (E) graph shows CdSe has high $\alpha \approx 9\times10^4$ cm^{-1} for higher energy photons range. Also, the direct optical energy bandgap can be derived by

$$(\alpha E)^2 = A\left(E - E_{gap}\right) \tag{4.3}$$

Where α, E, A, E_{gap} represent absorption coefficient, photon energy, proportionality constant, and energy bandgap respectively. $(\alpha.E)^2$ vs. E plot shows a linear dependence which can normally confirmed that CdSe is a direct bandgap semiconductor. Also, we calculated a direct optical bandgap of ~1.72eV by extrapolating the straight line on the energy axis. The optical data of 1um CdSe film that was deposited at 350ºC is shown by Figure 4-15.

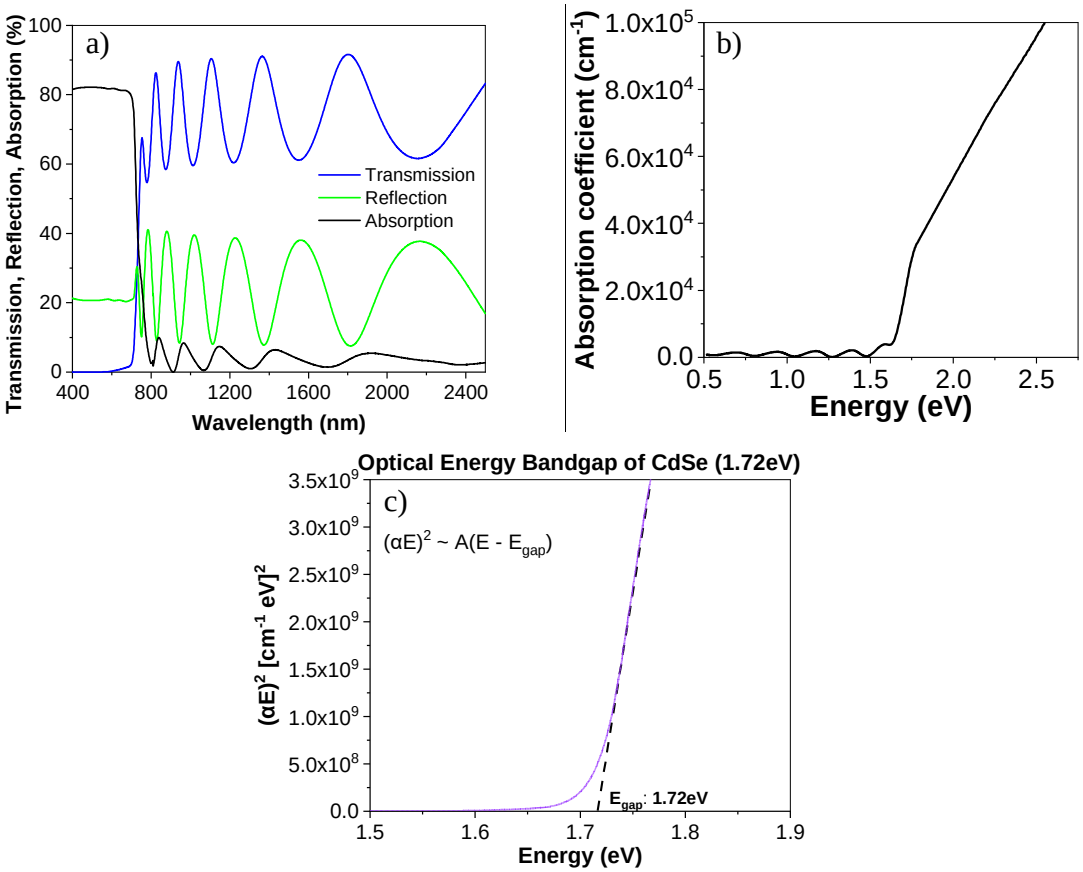
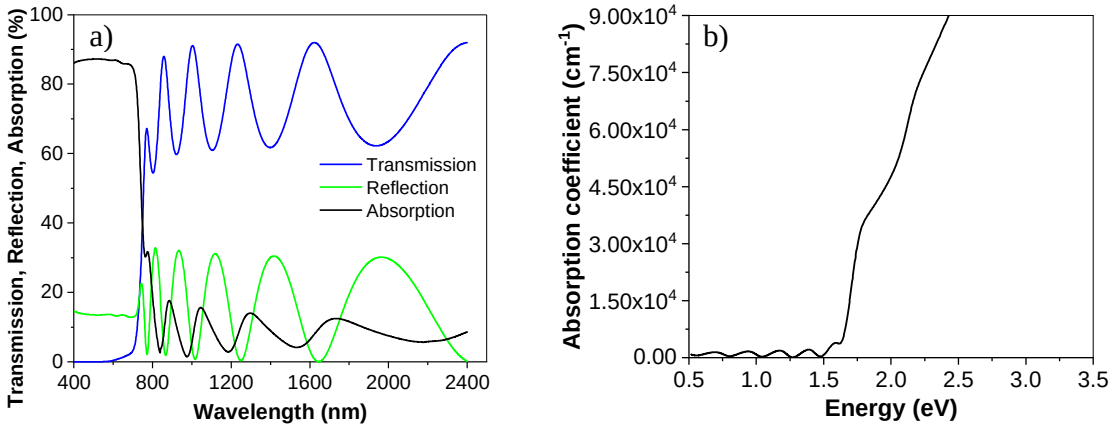


Figure 4-15 Optical data of 1um CdSe film at 350ºC, A) Transmission, Reflection, and Absorption, B) Absorption coefficient, C) Energy bandgap (1.72eV) [25].

The optical data of 1um CdSe film that was deposited at 300ºC is shown by Figure 4-16.



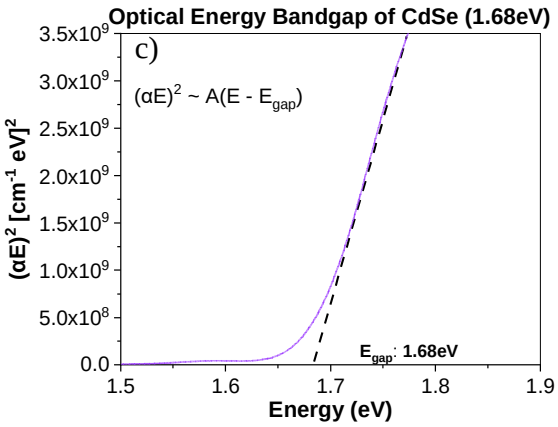


Figure 4-16 (continued) Optical data of 1um CdSe film at 300ºC, A) Transmission, Reflection, and Absorption, B) Absorption coefficient, C) Energy bandgap (1.68eV).

4-5-2 Grain enhancement on CdSe thin films

Grain enhancement experiment was performed on CdSe films for different substrates, annealing temperature, annealing time, and film thicknesses. In following parts, we will report the results in depth. A 2%wt of $CdCl_2$ solution in water was used for $CdCl_2$ heat treatment. All $CdCl_2$ experiment was performed using spin-coating technique.

4-5-2-1 CdSe with Se flux (CdSe:Se)

We studied the effect of $CdCl_2$ treatment of CdSe film with Se flux which was deposited on micro glass substrate. Two identical samples were prepared, then $CdCl_2$ treatment was performed on one of them under following conditions.

Device structure: Glass/CdSe:Se/$CdCl_2$

CdSe with Se flux: 400ºC (Annealing temperature), 1um (Film's thickness), 2:10Å/Sec (Deposition rate for CdSe and Se).

$CdCl_2$: 2%Wt (Solution concentration), 30min (Annealing time), N_2 (Nitrogen ambient).

Table 4-1 $CdCl_2$ treatment on CdSe with Selenium flux.

Sample	S1	S2
Annealing Temp	No	400ºC
Grain size	~0.3µm	~7-8µm

The SEM image of CdSe:Se film is shown in Figure 4-18.

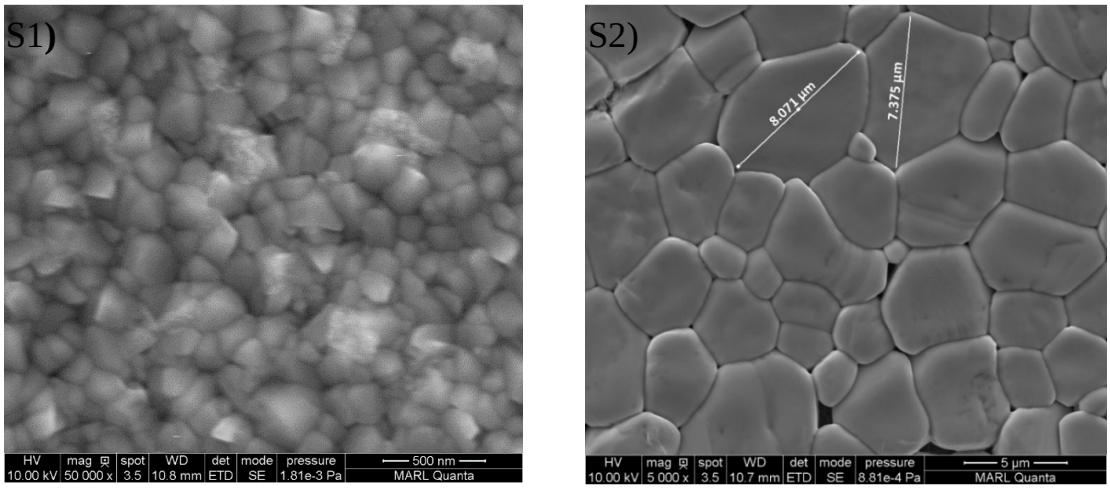


Figure 4-17 SEM for S1: as-deposited (0.3µm) and S2: after $CdCl_2$ annealing (7-8µm).

The grain size of as-deposited CdSe is around 0.3µm. It increased significantly after annealing up to 8µm. The largest grain enhancement (~27X larger) was achieved on glass for CdSe with Se flux. Grain enhancement is strongly depend of substrate. CdSe films deposited on NiO_x, PTAA, and ZnTe flaked off under $CdCl_2$ treatment.

4-5-2-2 Effect of annealing temperature

In this section, I have done a systematic study on grain enhancement of CdSe thin films under different annealing temperature on FTO/CdS substrate. Where FTO and CdS are fluorine doped thin oxide and cadmium sulfide respectively. We have used CdS as electron transport layer (ETL) because its conduction band matches well with conduction band of CdSe. We fabricated four identical samples, then $CdCl_2$ treatment was performed under following conditions.

Device structure: FTO/CdS/CdSe/CdCl2

CdS: 200ºC, 1µm

CdSe: 400ºC, 0.5µm

CdCl2: 2%Wt, 2h, N_2

Table 4-2 $CdCl_2$ treatment on CdSe thin films under different annealing temperature.

Sample number	S3	S4	S5	S6
Annealing Temp	No	400ºC	450ºC	500ºC
Grain size	~0.3µm	~1.2 µm	~1.4 µm	~1.7 µm

The SEM image of CdSe film is shown in Figure 4-18.

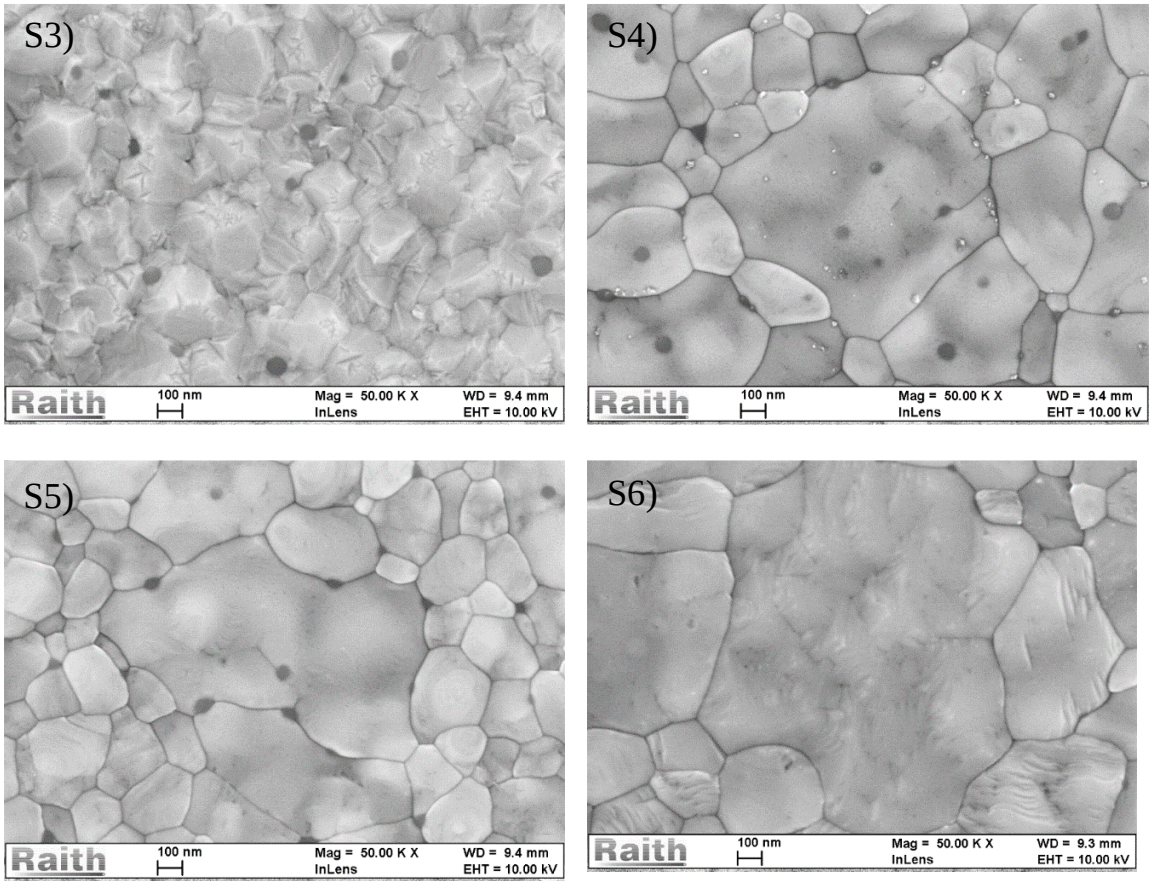


Figure 4-18 Effect of annealing temperature on CdSe film grain sizes.

The grain size of as-deposited CdSe is around 0.3µm. Grains increase significantly after annealing. The grain size for 0.5µm CdSe on FTO/CdS substrate under 2h $CdCl_2$ at 500ºC is about 1.7µm.

4-5-2-3 Cross section SEM image of CdSe film

One of the purpose of $CdCl_2$ treatment is improving the grain size not only on the top surface, but also all over the place in the depth of film. The SEM cross section images for sample S6 is shown in Figure 4-19. This image confirms that $CdCl_2$ penetrates perfectly into the depth of 0.5µm.

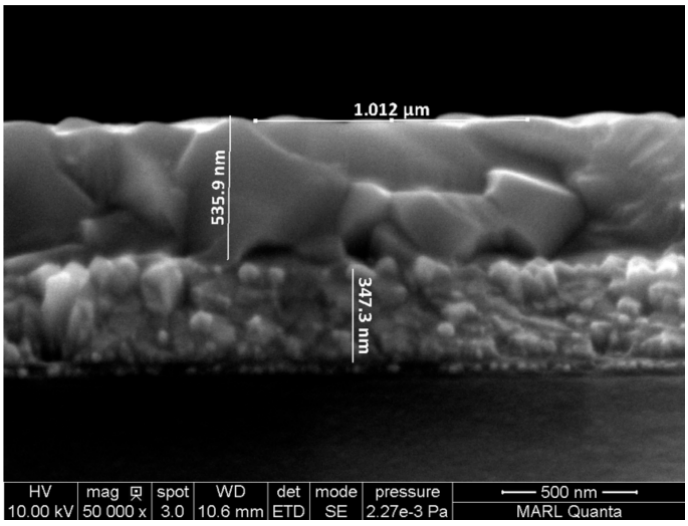


Figure 4-19 SEM cross section for 0.5um CdSe after $CdCl_2$ treatment [25].

4-5-2-4 Effect of CdSe film's thickness on grain enhancement

This study reveals the effect of CdSe film's thickness and $CdCl_2$ treatment on CdSe grain sizes and surface morphology. We prepared CdSe samples with four different thicknesses (two from each), then $CdCl_2$ treatment was performed on one sample from each categories. The experiment design is shown here.

Device structure: FTO/CdS/CdSe/$CdCl_2$

CdS: 200ºC, 100nm

CdSe: 400ºC, 0.5µm, 1µm, 2µm, 3µm

$CdCl_2$: 2%Wt, 500ºC, 30min, N_2

Table 4-3 $CdCl_2$ treatment on CdSe films with different thicknesses.

	As-deposited				After grain enhancement			
Sample number	S7	S8	S9	S10	S11	S12	S13	S14
Thickness [µm]	0.5	1	2	3	0.5	1	2	3
Grain sizes [µm]	0.3	0.5	0.7	0.9	1	1.3	1.5	1.9

The SEM images for as-deposited CdSe films with four different thicknesses are shown in Figure 4-20. As-deposited CdSe film with 0.5µm thickness has smaller grain size about 0.3µm. While film's surface becomes rough for thicker film (3µm) while grain size also increases up to 0.9um.

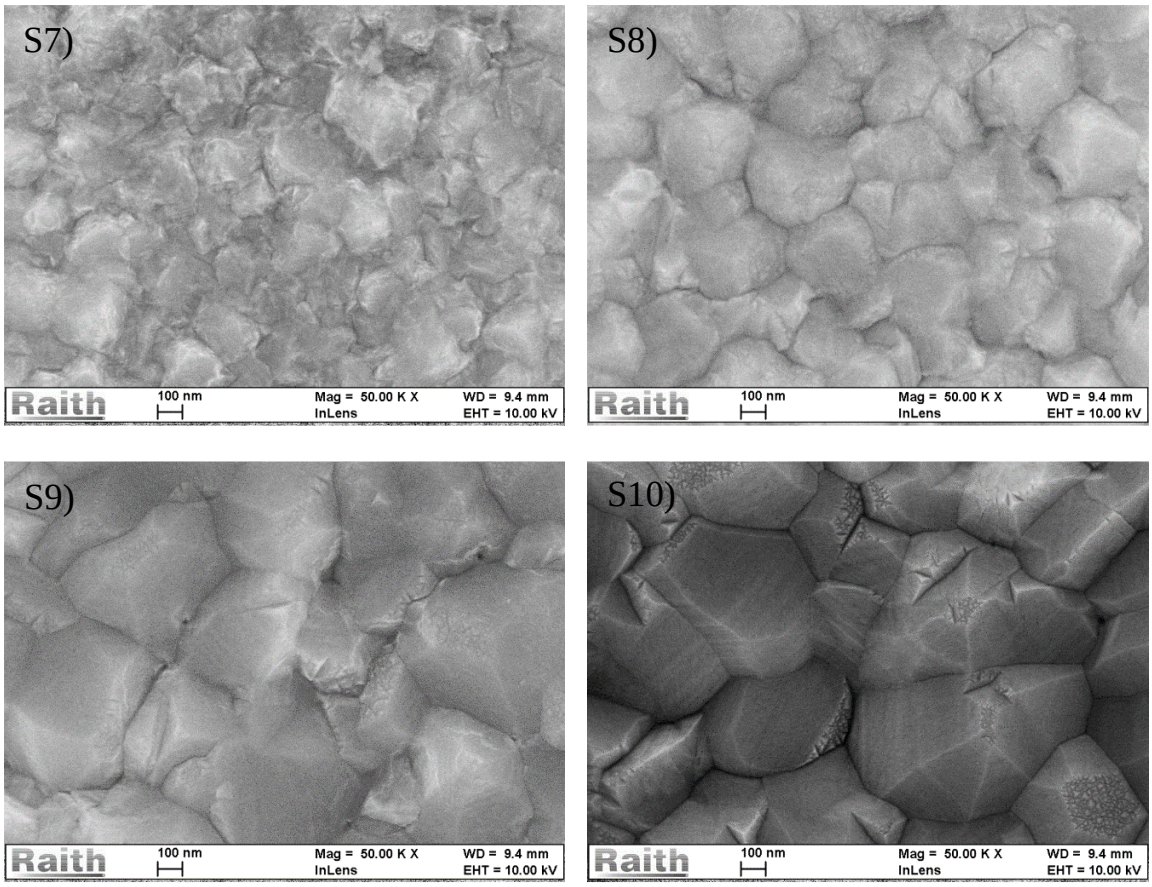


Figure 4-20 Effect of CdSe film's thickness on CdSe grain sizes and surface morphology [25].

The SEM images of CdSe films after annealing with four different thicknesses are shown in Figure 4-21.

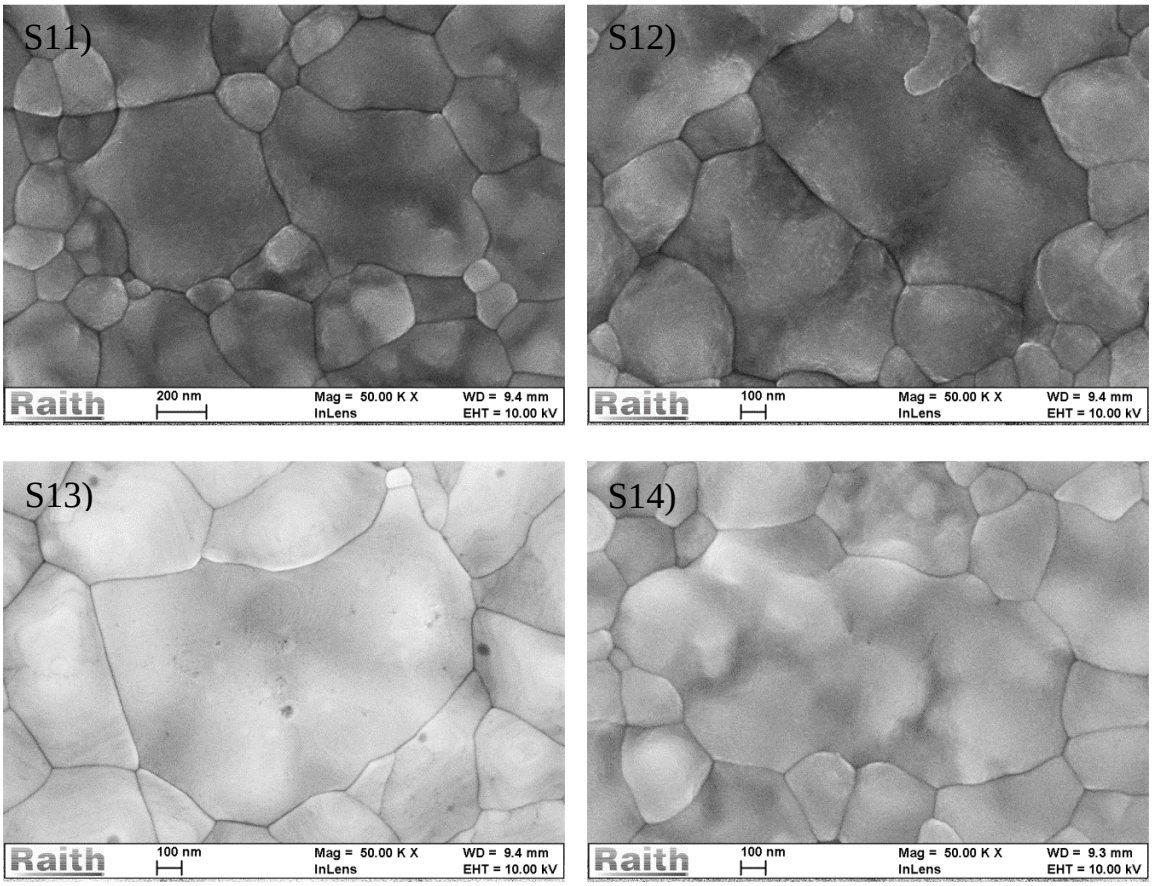


Figure 4-21 Effect of CdSe film's thickness and $CdCl_2$ treatment on CdSe grain sizes and surface morphology [25].

Grain size for 0.5um CdSe film after annealing is 0.9um. While grain size for 3um CdSe film after annealing is in the range of 1.9um. SEM images clearly show that films surface become flat and smooth after grain enhancement.

4-5-2-5 Electrical properties of CdSe thin films before and after grain enhancement

The electron mobility and carrier concentration of CdSe films were measured using SCLC [26] as described in Chapter 3. We used CdS and PCMB as two electron transport layer to

make good ohmic contacts on both sides. The experiment design and device structure for SCLC are provided (Figure 4-22).

Device structure: FTO/CdS/CdSe/$CdCl_2$/PCBM/Al

CdS: 200ºC, 100nm

CdSe: 400ºC, 0.5µm, 1µm, 2µm, 3µm

$CdCl_2$: 2%Wt, 500ºC, 30min, N_2

PCMB: 20mg/ml, 2000rpm, 60Sec, 150C, 15min

Al: 100nm

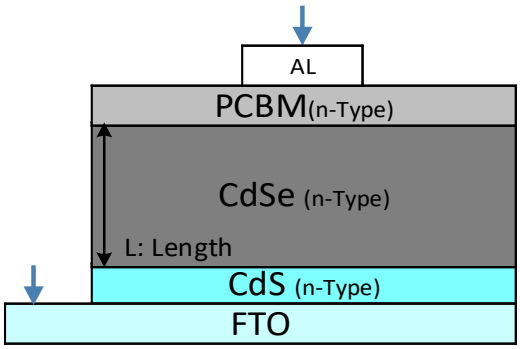


Figure 4-22 Device structure for SCLC experiment on CdSe film.

The current density vs. voltage and voltage square characteristic for as-deposited and after grain enhancement CdSe films with four different thicknesses are shown in Figure 4-23. As we described before, mobility can be calculated from the slop of J vs V^2.

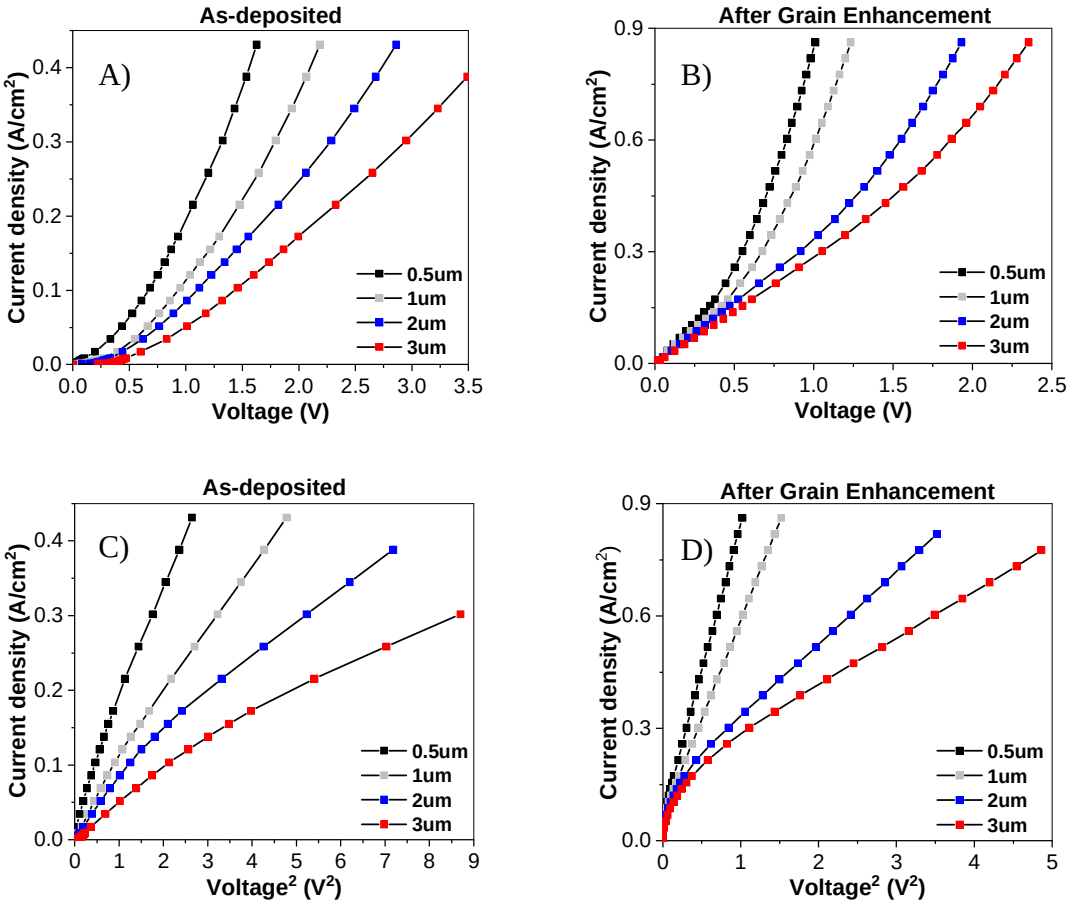


Figure 4-23. I-V curves from SCLC experiment to measure mobility and carrier concentration of as-deposited and after grain enhancement CdSe films under four different thicknesses [25].

The highest mobility was 3.5 $cm^2/V.S$ for 3µm film after grain enhancement since it has larger grain compare to others. And the lowest mobility is 0.02 $cm^2/V.S$ for 0.5µm as-deposited film due to smaller grain compare to other cases (Table 4-4).

Table 4-4 Mobility and carrier concentration for as-deposited and after grain enhancement of CdSe film.

	As-deposited				After grain enhancement			
Sample number	S7	S8	S9	S10	S11	S12	S13	S14
Thickness [µm]	0.5	1	2	3	0.5	1	2	3
Grain sizes [µm]	0.3	0.5	0.7	0.9	1	1.3	1.5	1.9
Mobility [$cm^2/V.S$]	0.018	0.084	0.366	0.624	0.098	0.535	1.446	3.525
Carrier concentration [cm^{-3}]	2.21×10^{14}	1.55×10^{14}	6.36×10^{13}	3.99×10^{13}	3.32×10^{14}	2.49×10^{14}	1.24×10^{14}	8.60×10^{13}

Figure 4-24 shows, mobility increases and carrier concentration decreases by increasing the film thickness. Also it reveals that mobility and carrier concentration are higher for after grain enhancement CdSe film compare to as-deposited.

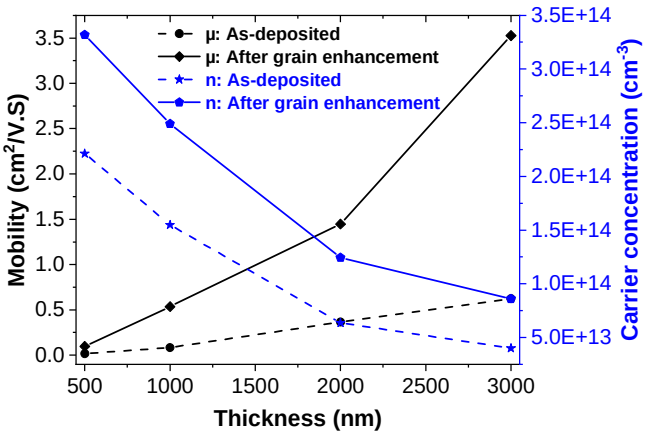


Figure 4-24 Mobility and carrier concentration of as-deposited and after grain enhancement of CdSe thin films.

4-5-2-6 Effect of post-deposition selenization on grain enhancement

This study reveals the effect of post-deposition selenization on CdSe grain sizes and surface morphology. We prepared four CdSe samples with 1um thickness. Then post selenization was performed under different time (Table 4-5).

Device structure: Glass/CdSe/Selenization/Aluminum bars

CdSe: 400ºC, 1um

Selenization: Tsub: 450ºC, Tboat: 327ºC, N_2

Selenization Time: No, 30 min, 60 min, 120min

Table 4-5 Post-deposition selenization on CdSe films for different time.

	As-deposited	After post-deposition selenization		
Sample number	S15	S16	S17	S18
Selenization time	…	30min	60min	120min
Grain sizes	0.3µm	3 µm	3.8 µm	5.7 µm

SEM measurements were conducted to investigate the grains. SEM image of as-deposited sample shows small grain about 0.3µm. The surface microstructure is found to be affected due to higher surface thermal energy and the grain size gets larger by increasing selenization time. For example sample has 19X larger grain after 120min selenization compare to as-deposited sample (Figure 4-25).

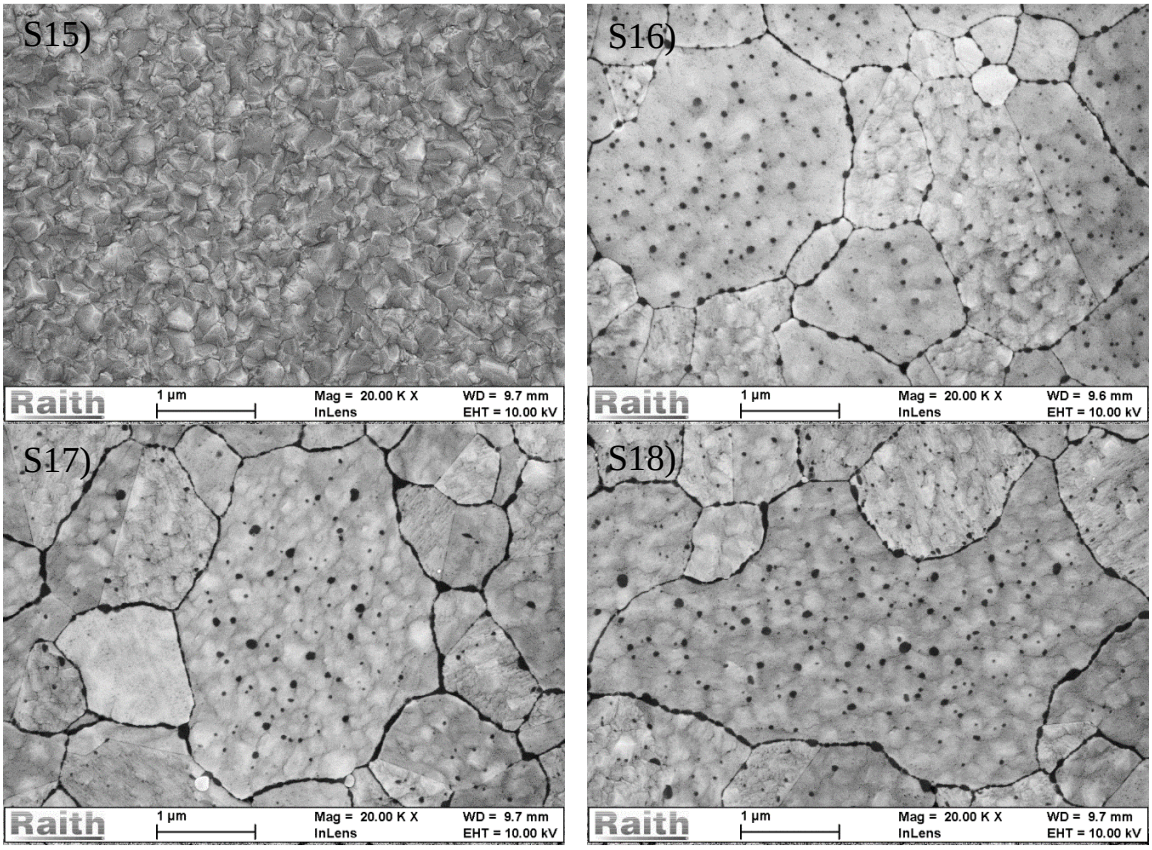


Figure 4-25 SEM images for as deposited and after post selenization of CdSe thin films.

4-5-2-7 Electrical properties of CdSe thin films before and after post-deposition selenization

The photoconductivity and mobility-lifetime product for as-deposited and post-selenized CdSe samples were measured as explained in Chapter 3. Two aluminum bars were made on glass/CdSe structure to measure current vs. voltage characteristic under dark and light illumination (AM1.5) inside a dark box. Current was measured for a range of voltage between

-50V to +50V. Table 4-6 summarizes electrical properties including light to dark conductivity ratio (σ_{Light} / σ_{Dark}), photoconductivity ($\Delta\sigma = \sigma_{Light} - \sigma_{Dark}$), and mobility-lifetime product ($\mu\tau$). Selenization improved the photo-conductivity from 2.94×10^{-4} $(\Omega.cm)^{-1}$ to 1.2×10^{-3} $(\Omega.cm)^{-1}$ for as-deposited and 120 minutes post-selenized samples respectively (~36 times larger). Also it increased the light-to-dark conductivity ratio from 79 to 1.2×10^{6} for as-deposited and 120 minutes post-selenized samples respectively (~1.5×10^{4} times larger). This study reveals that $\mu\tau$ increases from 1.37×10^{-6} cm^2/V to 5.62×10^{-6} cm^2/V as selenization time increases.

Table 4-6 Electrical properties of as-deposited and Post-selenized CdSe samples.

	As-deposited	After post-deposition selenization		
Sample number	S15	S16	S15	S16
Selenization time	…	30min	60min	120min
Grain sizes	0.3µm	3µm	3.8 µm	5.7µm
$\sigma_{Light}/\sigma_{Dark}$	79	2.03×10^{5}	8.28×10^{5}	12.05×10^{5}
$\Delta\sigma = \sigma_{Light}-\sigma_{Dark}$	2.94×10^{-4} $\Omega.cm^{-1}$	7.92×10^{-4} $\Omega.cm^{-1}$	1.00×10^{-3} $\Omega.cm^{-1}$	1.21×10^{-3} $\Omega.cm^{-1}$
$\mu\tau$	1.37×10^{-6} cm^2/V	3.68×10^{-6} cm^2/V	4.65×10^{-6} cm^2/V	5.62×10^{-6} cm^2/V

Dark and light resistivity, and mobility-lifelime product ($\mu\tau$) of CdSe films as a function of selenization time are shown in Figure 4-26 and Figure 4-27 respectively.

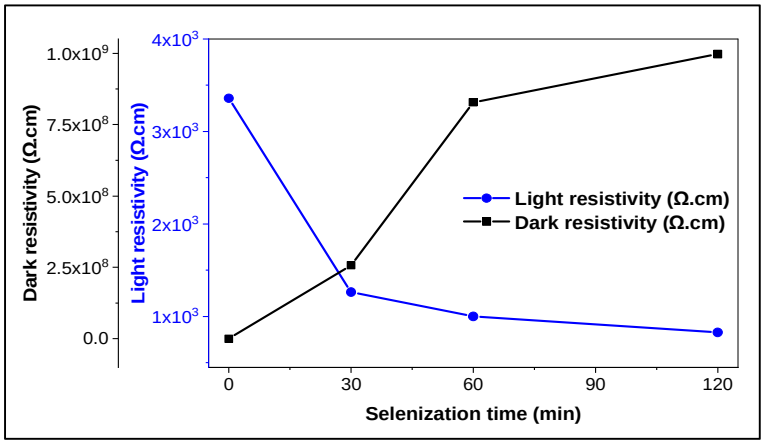


Figure 4-26 Dark and light resistivity of CdSe films under post-selenization experiment.

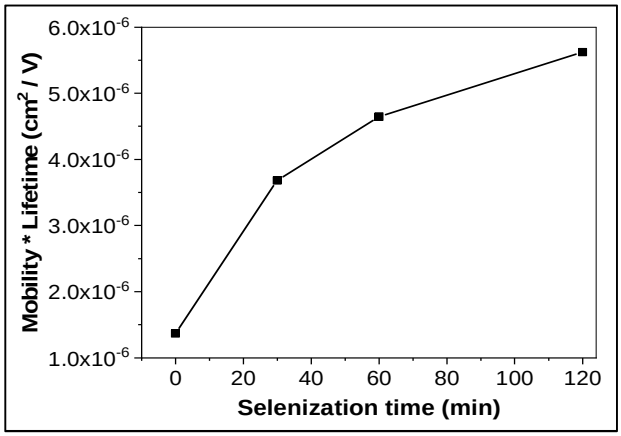


Figure 4-27 Mobility-lifelime product (μτ) of CdSe films under post-selenization experiment [25].

4-5-2-8 Sub-gap QE on CdSe film

Polycrystalline materials have tail state near the conduction and valence bands due to crystalline disorder. Sub-gap QE is a useful technique to measure these tail states which provides essential electronic properties of the semiconductors [27]. Figure 4-28 shows the absorption coefficient of CdSe as a function of photon energy. Region (A) is due to transients from valance band to conduction band (band-to-band transients). In region (B) by decreasing the photon energy bellow the bandgap (1.72eV), α drops due to tail states transient. Finally, region (C), deep defects transitions are dominate at very low energy [28]. The, α as a function of energy using sub-gap QE can be derived by following equations.

$$N_0(\lambda) = Vout_{Ref}(\lambda)/QE_{Ref}(\lambda) \quad (4.3)$$

$$QE_{Sample}(\lambda) = Vout_{Ref}(\lambda)/N_0(\lambda) \quad (4.4)$$

$$\alpha(\lambda) = \alpha(@720nm) \times QE_{Sample}(\lambda) \quad (4.5)$$

A silicon reference solar cell was used to measure number of incident photons (N_0). Where, $Vout_{Ref}$, and QE_{Ref} are output signal and quantum efficiency of the reference Silicon cell respectively. The QE_{Sample} is the quantum efficiency of the CdSe sample.

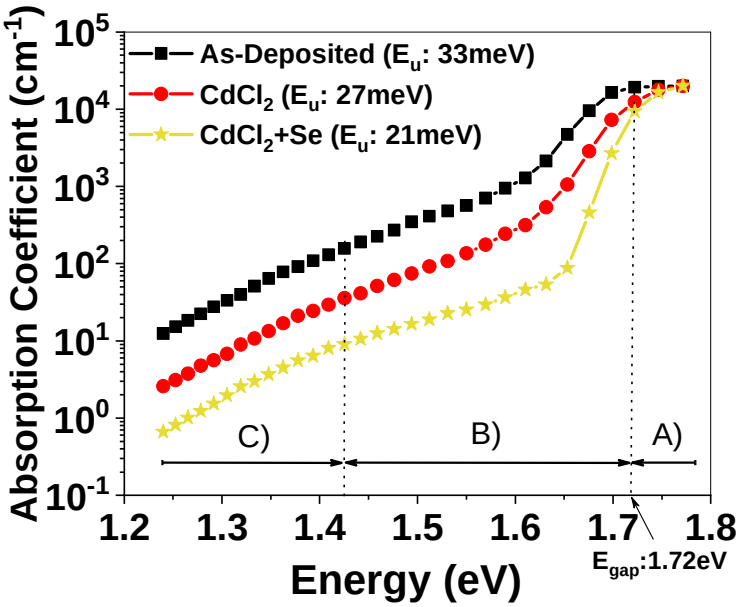


Figure 4-28 Absorption coefficient vs. energy for three samples including As-Deposited, $CdCl_2$ Treated, and $CdCl_2$ Treated + Selenized samples. Region (A) band-to-band transients, Region (B) tail states transient and Region (C) deep defects transitions [25].

The Urbach energy of tail states, E_u, which is deduced from the equation:

$$\alpha = \alpha_0 \exp(-\frac{E - E_c}{E_u}) \tag{4.6}$$

Where E_c is energy of conduction band. The Urbach energy is also reduced with selenization, and has a value of 21meV for the best film. This value is in the same range for other efficient photovoltaic materials such as perovksites [29].The figure also shows that at lower energies, there is flattening of the curve, indicating the presence of midgap states, and that selenization has also reduced the density of such states. This, of course is the reason why the electron ($\mu\tau$) product increased after selenization.

4-5-2-9 EDS results on CdSe thin films

As we discussed in chapter 3, EDS is a useful tool to provide technical information about chemical composition of material. In this section, we have shown EDS results on different

experiments. We discovered that, one of the key steps to perform accurate EDS analysis, is applying high enough acceleration voltage.

First experiment was carried out on CdSe films where deposited on silicon substrate. The EDS was measured under four different voltages as 5KeV, 8KeV, 10KeV, and 15KeV.

Device structure: Si/CdSe

CdSe: 300ºC, 500nm

Table 4-7 EDS on CdSe films under different accelerating voltages.

Sample number	Voltage	Se / Cd [Atomic %]
CdSe-08	5KeV	0.930
CdSe-08	8KeV	0.943
CdSe-08	10KeV	0.993

As we can see, Se/Cd under 10KeV is almost close to 1 that shows our CdSe film is stoichiometric. Also there is a limit for acceleration voltage depends on film thickness, because beyond that limit, electron penetrates more into the depth and x-ray comes off from the substrate which can affect our measurement. Figure 4-29 shows EDS spectrums of CdSe films on Si substrate under several acceleration voltages. Si peak which is corresponding to Si substrate is visible at higher voltage (15kev). So 10KeV is well enough for 500nm CdSe film.

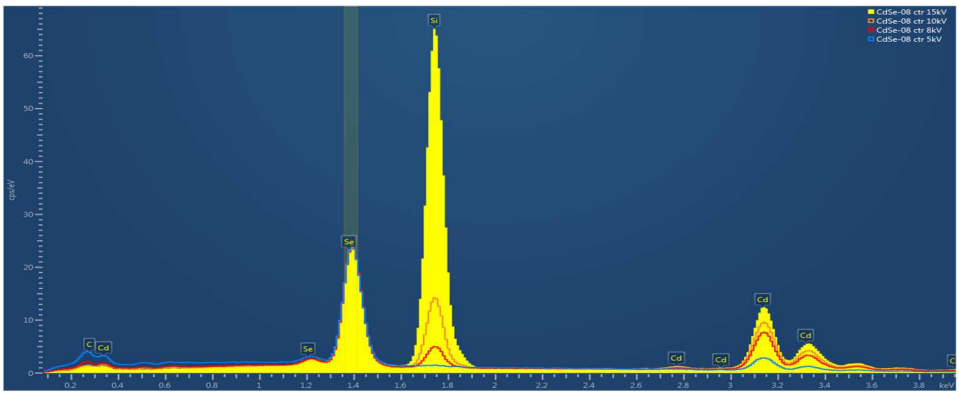


Figure 4-29 EDS spectrum of CdSe film on Si substrate.

Second, experiment was carried out on thicker CdSe films where deposited at higher substrate temperature. The EDS was measured under three different voltages as 8KeV, 10KeV, and 15KeV.

Device structure: Si/CdSe

CdSe: 400ºC, 750nm

Table 4-8 EDS on CdSe films under different accelerating voltages.

Sample number	Voltage	Se / Cd [Atomic %]
CdSe-10	8KeV	0.950
CdSe-10	10KeV	0.975
CdSe-10	15KeV	1.000

Table 4-8 shows Se/Cd for 750nm CdSe film under 15KeV is perfect equal to 1.

Third experiment was performed on CdSe films with and without $CdCl_2$ treatment. 500nm CdSe film was deposited on glass substrate at 300C. $CdCl_2$ treatment was carried out on one sample at 385ºC for 30min. The EDS was measured under 10KeV.

Device structure: Glass/CdSe/CdCl2

CdSe: 300ºC, 500nm

CdCl2: 385ºC, 30min

Table 4-9 EDS on CdSe films for with and without CdCl2 treatment.

Sample number	CdCl2	Se / Cd [Atomic %]
CdSe-30-P4	No	0.980
CdSe-30-P2	Yes	0.979

Se to Cd ratio of CdSe films for as-deposited and after $CdCl_2$ treatment is almost identical.

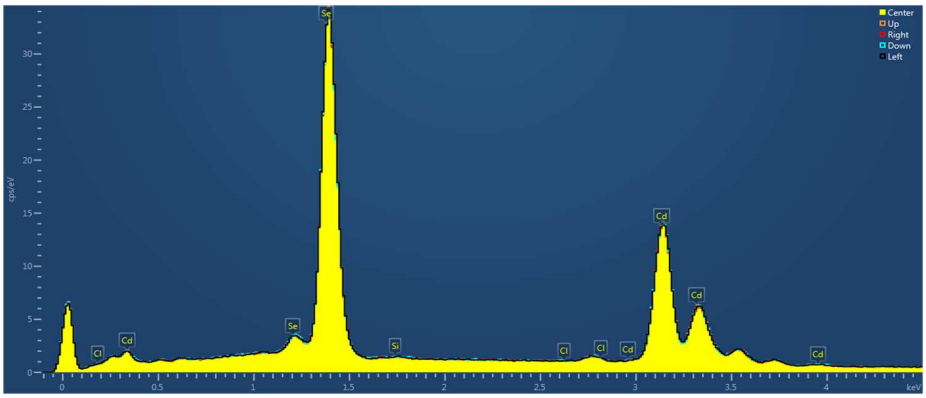


Figure 4-30 EDS spectrum of CdSe film on Glass substrate.

Next, we performed EDS analysis on a standard stoichiometric CdSe wafer. Results also confirmed that to perform an accurate EDS measurement on CdSe film and wafer, 20KeV acceleration voltage under Se K line is required.

Table 4-10 EDS on CdSe wafer under different voltage and Se line type.

Voltage	Line Type	Se / Cd [Atomic %]
10KeV	Se L line	0.941
20KeV	Se L line	0.953
20KeV	Se K line	0.995

Se to Cd ratio of CdSe wafer under 20KeV using Se K line is almost close to one (0.995).

In addition, EDS analysis was conducted to investigate the effect of $CdCl_2$ treatment on CdSe films deposited under selenium flux. 1µm CdSe film was deposited on FTO/CdS substrate at 450ºC. CdSe films were deposited with and without selenium flux (1Å/S). $CdCl_2$ treatment was carried out on one sample at 500ºC for 10h. The EDS was measured under 20KeV using Se K line.

Device structure: FTO/CdS/CdSe/$CdCl_2$

CdS:In: 300ºC, 30nm, Annealed: 400ºC, 30min, Air

CdSe : Se flux: 450ºC, 1µm, 5:0Å/S and 5:1Å/S

CdCl2: 500ºC, 10h

The device parameters and EDS results for this experiment are shown in Table 4-11 and Figure 4-31. As we can see samples are almost stoichiometric.

Table 4-11 EDS on CdSe films deposited under selenium flux and $CdCl_2$ treatment.

Device	CdSe : Se	$CdCl_2$	Se / Cd [Atomic %]
823L	5:0Å/S	No	1.023
822R	5:0Å/S	Yes	1.007
834R	5:1Å/S	No	1.003
834L	5:1Å/S	Yes	1.013

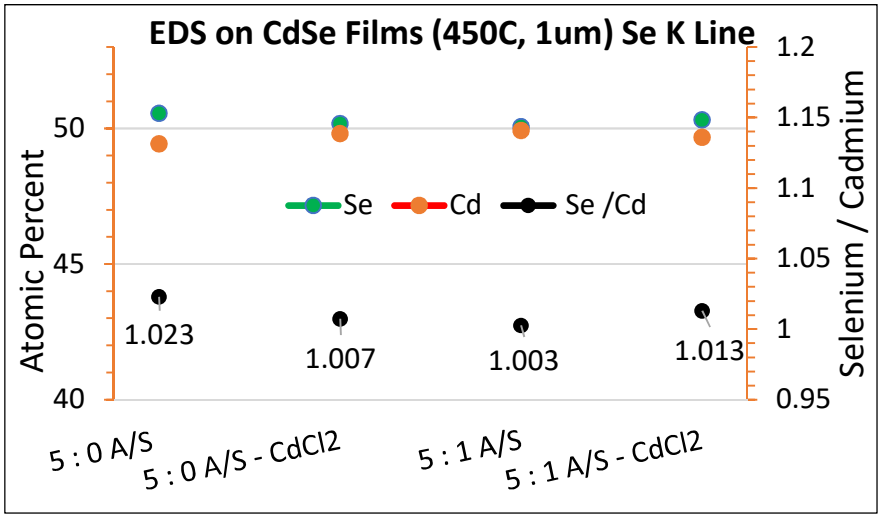


Figure 4-31 EDS on CdSe films deposited under selenium flux and $CdCl_2$ treatment.

Se to Cd ratio of CdSe all different films including with and without $CdCl_2$ and selenium flux under 20KeV using Se K line is almost close to one.

Finally, EDS analysis was carried out to study the effect of post-annealing on CdSe films deposited under selenium flux. 1µm CdSe film was deposited on FTO/CdS substrate at 300ºC without 2Å/S selenium flux. Post-annealing was done on one sample at 450ºC for 2h. The EDS was measured under 20KeV using Se K line.

Device structure: FTO/CdS/CdSe/Anneal

CdS:In: 300ºC, 30nm, Annealed: 400ºC, 30min, Air

CdSe: Se flux: 300ºC, 1µm, 5:0Å/S and 5:2Å/S

$CdCl_2$: 450ºC, 2h

The device parameters and EDS results for this experiment are shown in Table 4-12 and Figure 4-32. As we can see samples are almost stoichiometric.

Table 4-12 EDS on CdSe films deposited under selenium flux and post-annealing.

Device	CdSe : Se	Anneal	Se / Cd [Atomic %]
851L	5 : 0 Å /S	No	1.011
851R	5 : 0 Å /S	Yes	1.021
853R	5 : 2 Å /S	No	1.005
853L	5 : 2 Å /S	Yes	1.009

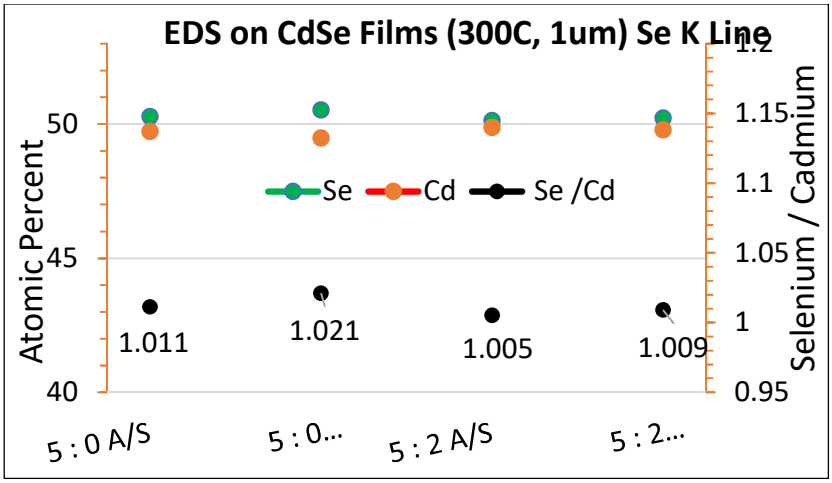


Figure 4-32 EDS on CdSe films deposited under selenium flux and post-annealing.

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CHAPTER 5. CADMIUM SELENIDE HETEROJUNCTION SOLAR CELLS DESIGN, FABRICATION AND OPTIMIZATION

5-1 Introduction

In this chapter, I will discuss how to design CdSe device using appropriate heterojunction (modified type two) solar cells. Fabrication steps, device optimization and characterization of CdSe cells are provided.

5-2 Correct solar cell device structure

As we explained in chapter two, solar cell devices can be made in N-i-P or P-i-N structure in both superstrate or substrate configuration. In this project, I have worked on two main heterojunction configuration as NP superstrate or PN substrate cells Figure 5-1.

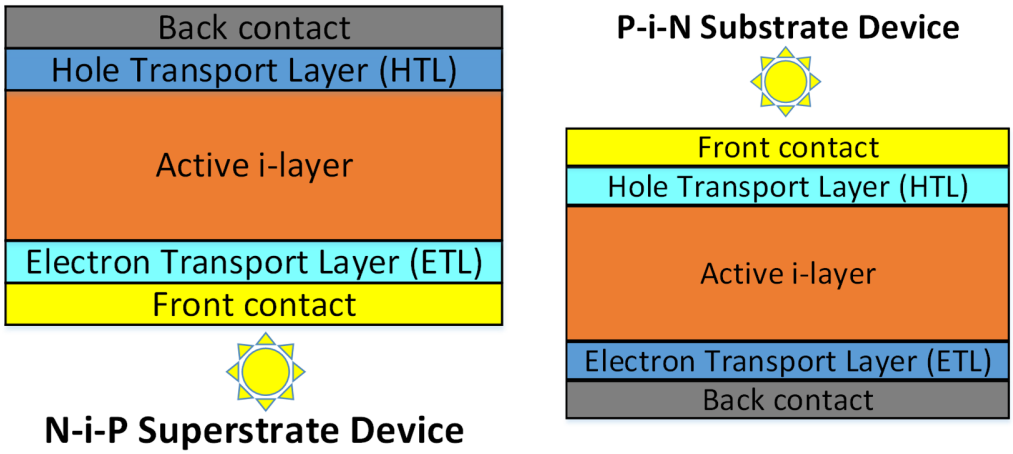


Figure 5-1 Type two heterojunction CdSe solar cells. NP superstrate (left), PN substrate (right).

As we know, CdSe is an n-type and direct bandgap semiconductor. So, electron transport layer (ETL) prevents hole recombination at n+/n(CdSe) interface and hole transport layer (HTL) prevents electron recombination at n(CdSe)/p^+ interface. Basically, ETL is an n-type layer like Cadmium Sulfide (CdS), Phenyl C61 butyric acid methyl ester (PCBM), Titanium-di-oxide (TiO_2), and Zinc Oxide (ZnO) etc. Similarly, HTL is a p-type layer such as Poly(3-hexylthiophene-2,5-diyl) (P3HT), Poly[bis(4-phenyl) (2,4,6-trimethylphenyl) amine] (PTAA),

polystyrene sulfonate (PEDOT), zinc telluride (ZnTe), zinc selenide (ZnSe), Nickel (II) Oxide (NiO), heavily doped p-plus amorphous silicon carbide (p^+-a-SiC) etc.

5-3 Electron and hole transport layers fabrication

Some of above mentioned ETL and HTL are organic layers and they need to be spin-coated on substrate or device like PCMB, TiO_2, P3HT, PTAA, and PEDOT. The procedure for making organic layers are explained in details. Some of ETL and HTL are inorganic materials such as CdS, ZnO, ZnTe, ZnSe, NiOx, which are deposited using physical evaporation techniques like thermal evaporation, e-beam and sputtering. Also p^+-a-SiC as heavily-doped HTL is deposited using plasma enhanced chemical vapor deposition (PECVD). In some cases, to achieve better Ohmic contact, we can dope CdS with Indium and ZnO using Aluminum in order to increase the conductivity.

PCBM layer: 20mg/ml PCBM in chlorobenzene was spin-coated at 2000rpm for 60Sec in nitrogen-filled glovebox, then it was annealed at 150C for 15min.

TiO_2 layer: TiO2 was fabricated on FTO substrate under following steps:

Solution-A was spin-coated at 6000rpm for 30sec in air, then it was annealed at 125°C for 5min. ***Solution-B*** was spin-coated at 6000rpm for 30sec in air, then it was annealed at 125°C for 10min. In the next step, sample was annealed at 550°C for 15min in air. Finally it was dipped in ***Solution-C*** while kept at 75°C for 30min.

Three solutions (A, B, and C) for fabrication of TiO_2 layer are listed here:

Solution-A (0.15 Molar): 141µL TDB + 1359µL 1-Butanol

Solution-B (0.3 Molar): 282µL TDB + 1218µL 1-Butanol

Solution-C: 50mL DI water + 1140µL Titanium tetrachloride ($TiCl_4$)

TDB: titanium diisopropoxide bis (acetylacetonate)

P3HT layer: 15mg/ml P3HT in chlorobenzene was spin-coated at 1000rpm for 60Sec in nitrogen-filled glovebox, then it was annealed at 150°C for 15min.

PEDOT/PSS layer: PEDOT/PSS was spin-coated at 1000rpm for 40Sec in air. Then it was annealed at 200°C for 15min.

PTAA: 10mg/ml PTAA in Toluene was spin-coated at 3000rpm for 60Sec in nitrogen-filled glovebox, then it was annealed at 150°C for 15min.

PTAA Doped: 10mg/ml PTAA in Toluene was doped in 7.5µl Lithium Salt plus 4µl t-BP. Next, it was spin-coated at 3000rpm for 60Sec in nitrogen-filled glovebox. Finally, it was annealed at 150°C for 15min.

5-4 NP superstrate devices

In this section, we proceeded to work on superstrate devices. As we explained in chapter 5-2, for superstrate devices light has to come from the bottom. We developed indium doped cadmium sulfide (CdS:In) and titanium dioxide (TiO_2) as bottom transparent contact.

5-4-1 NP superstrate device with FTO/TiO_2 on bottom

In this section, I will discuss the design, fabrication and optimization process of NP superstrate devices with FTO/TiO2 on the bottom. The device structure and energy band diagram are shown in Figure 5-2.

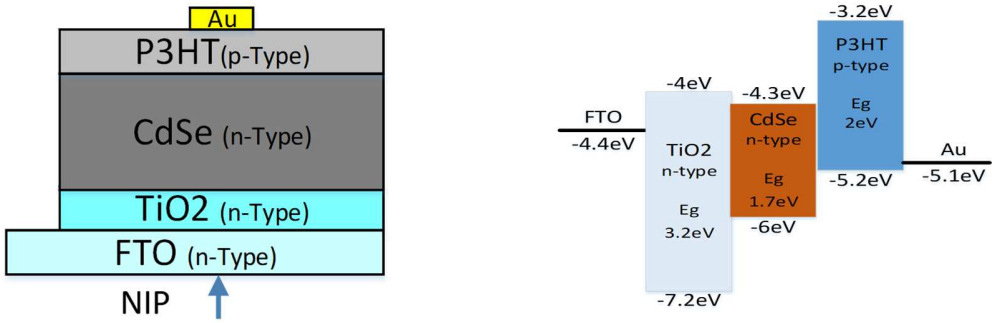


Figure 5-2 Device structure (Left) and energy band diagram (Right) of NP superstrate device.

Electron transport layer is TiO_2 layer on FTO substrate. CdSe film deposited using thermal evaporation at 400ºC for three different thickness 0.3µm, 0.5µm, and 1µm. 15mg/ml P_3HT as HTL was deposited using spin-coating. Finally a 45nm gold dots was deposited as top contact.

Device structure: FTO/TiO_2/CdSe/P_3HT/Au

TiO_2: 550ºC, 50nm

CdSe: 400ºC, 0.3-5Å/Sec, 0.3µm, 0.5µm, and 1µm

P3HT: 15mg/ml, 1000rpm, 60sec, 150C, 15min

Glod: 45nm

Results and discussion

The IV, QE and CV of devices are plotted in Figure 5-3. Open circuit voltage and short circuit current density for all three devices are listed in Table 5-1.

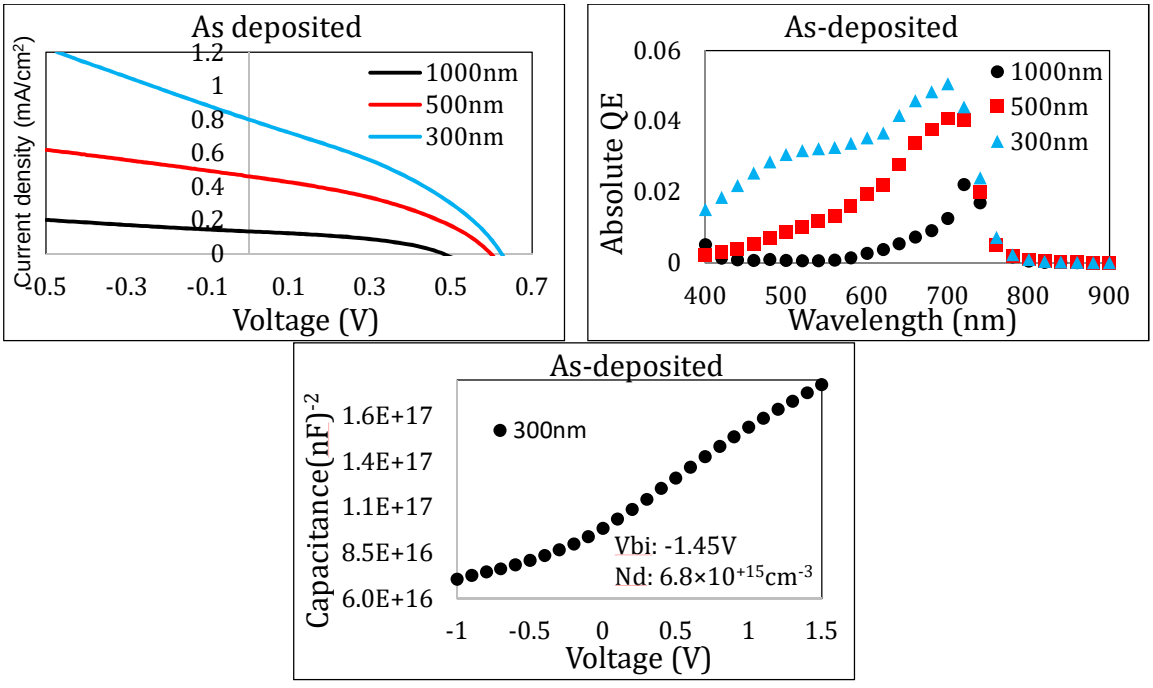


Figure 5-3 IV, QE, and CV for as-deposited NP superstrate with TiO_2 as ETL under different thicknesses.

In NP superstrate device, current increases by decreasing of film thickness and thinner device (0.3µm) gives higher current 0.8mA/cm^2 compare to other and open circuit voltage is about

0.6V. The C-V curve shows dopant density about $6.8\times10^{+15}$ cm^{-3} and built-in voltage of -1.45V.

Table 5-1 Open-circuit voltage and current density for as-deposited NP superstrate with TiO_2 as ETL under different thicknesses.

Device	Thickness(μm)	Voc and Jsc
E6-225	1	0.48V, 0.14mA/cm^2
E6-148	0.5	0.6V, 0.46mA/cm^2
E6-170	0.3	0.61V, 0.8mA/cm^2

In NP superstrate device, light is coming from n-side. For example, a high energy photon is absorbed in the area close to surface and electron-hole will be generated. Hole has to travel longer distance to be collected in p-side in thinker device compare to thinner device. So probability of collection is much higher in thinner device and this gives higher short circuit current (Figure 5-4).

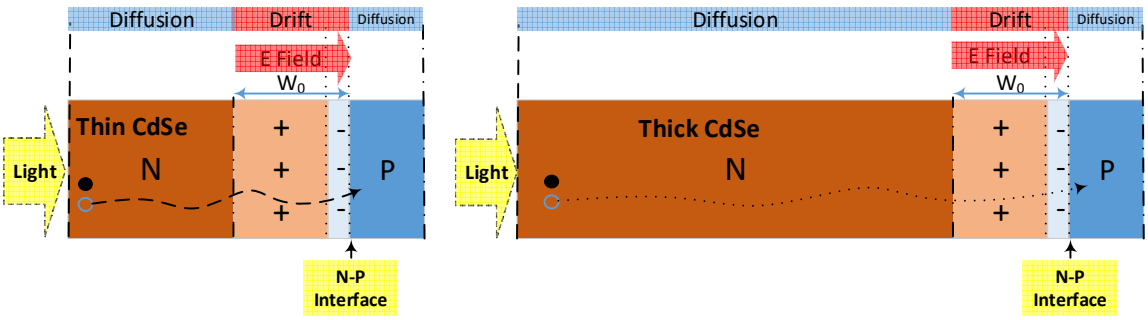


Figure 5-4 The collection of Hole as minority light generated carrier on the p-side in NP superstrate device, Thin device (Left) and Thick device (Right).

We have made the identical devices with $CdCl_2$ post-treatment. Grain enhancement was performed just after CdSe deposition.

Device structure: FTO/TiO_2/CdSe/P_3HT/Au

TiO_2: 550ºC, 50nm

CdSe: 400ºC, 0.3-5Å/Sec, 0.3µm, 0.5µm, and 1µm

$CdCl_2$: 2%Wt, 450ºC, 2h, N_2

P3HT: 15mg/ml, 1000rpm, 60sec, 150C, 15min

Glod: 45nm

Results and discussion

The IV, QE and CV of devices are plotted in Figure 5-5. Open circuit voltage and short circuit current density for all three devices are listed in Table 5-2.

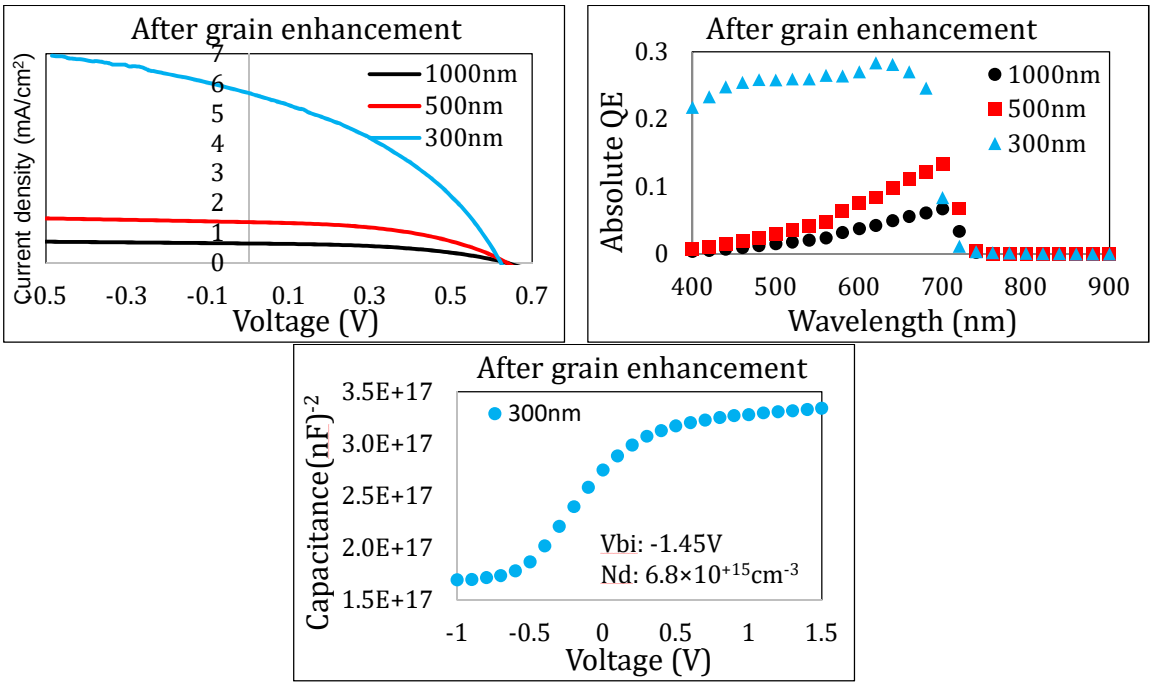


Figure 5-5 IV, QE, and CV for after grain enhanced NP superstrate with TiO_2 as ETL under different thicknesses.

Current density after grain enhancement increases significantly. Thinner device (0.3µm) shows 5.32mA/cm^2 after grain enhancement. So, the $CdCl_2$ treatment has a significant effect to increase the current density as it is observed from QE data.

Table 5-2 Open-circuit voltage and current density for after grain enhanced NP superstrate with TiO_2 as ETL under different thicknesses.

Device	Thickness(µm)	Voc and Jsc
E6-223A	1	0.66V, 0.65mA/cm^2
E6-149	0.5	0.64V, 1.37mA/cm^2
E6-171	0.3	0.61V, 5.32mA/cm^2

5-4-2 NP superstrate device with FTO/CdS on bottom

Cadmium sulfide (CdS) is a great ETL and makes very good ohmic contact with CdSe. In this section, we have made NP superstrate device with CdS as ETL. The device structure and energy band diagram of with FTO/CdS on the bottom are shown in Figure 5-6.

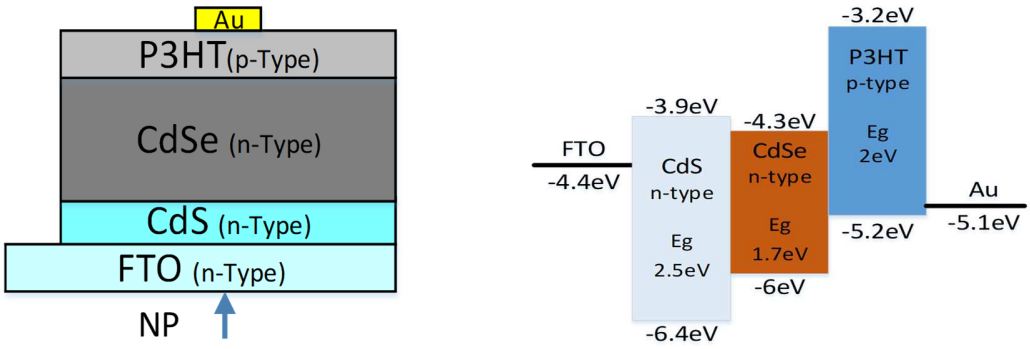


Figure 5-6 Device structure (Left) and energy band diagram (Right) of NP superstrate device.

5-4-2-1 Effect of annealing time

I have investigated the effect of $CdCl_2$ treatment annealing time on the device performance. The 100nm CdS was deposited using thermal evaporation at 200ºC on FTO substrate. Then 0.5µm CdSe film was deposited at 400ºC on CdS layer. $CdCl_2$ treatment was performed for times ranging from 2h to 10h. The top p-layer was P_3HT followed by a thick layer of gold contact.

Device structure: FTO/ CdS/CdSe/$CdCl_2$/P_3HT/Au

CdS: 200ºC, 100nm, 0.5Å/Sec

CdSe: 400ºC, 0.3-5Å/Sec, 0.5µm

$CdCl_2$: 2%Wt, 450ºC, 2h and 10h, N_2

P3HT: 15mg/ml, 1000rpm, 60sec, 150C, 15min

Glod: 45nm

Results and discussion

The IV, QE of devices are plotted in Figure 5-7. Open circuit voltage and short circuit current density for all three devices are listed in Table 5-3.

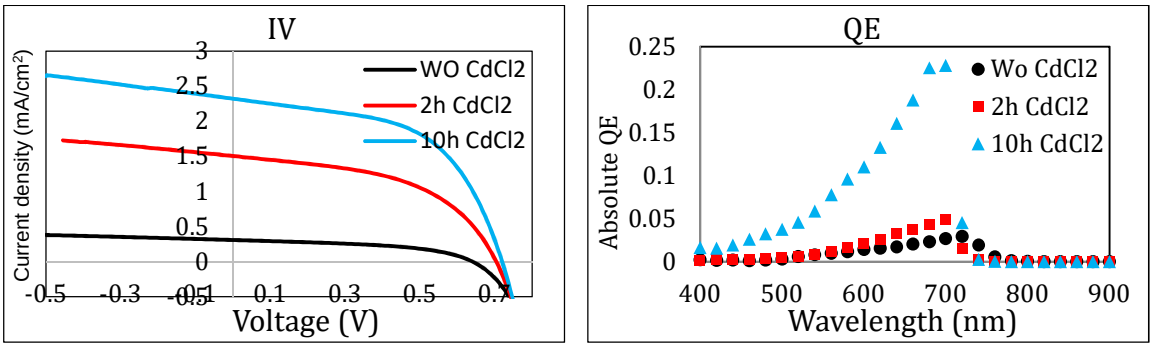


Figure 5-7 IV and QE for NP superstrate devices with CdS as ETL under different annealing time.

The current density increases by increasing the annealing time and current from QE is about 2.32mA.cm^2 for device that annealed for 10h. IV curves show a good voltage about 0.7V. As we explained before, $CdCl_2$ has a significant effect on grain growth and passivation of grain boundaries and prevent from recombination.

Table 5-3 Open-circuit voltage and current density for NP superstrate devices with CdS as ETL under different annealing time.

Device	Time_$CdCl_2$	Voc and Jsc
E6-367	No	0.64V, 0.31mA/cm^2
E6-365	2h	0.71V, 1.51mA/cm^2
E6-363	10h	0.72V, 2.32mA/cm^2

5-4-2-2 Effect of thickness

In order to optimize the device thickness, NP superstrate CdSe devices were made under two different thicknesses as 0.5µm and 1µm.

The 30nm thick CdS was deposited using thermal evaporation at 200°C on FTO substrate. Then CdSe films were deposited at 450ºC on CdS layer. $CdCl_2$ treatment was performed at 450ºC on both devices for 10h. The top p-layer was P_3HT followed by a thick layer of gold contact.

Device structure: FTO/CdS/CdSe/$CdCl_2$/P_3HT/Au

CdS: 200ºC, 30nm, 0.5Å/Sec

CdSe: 450ºC, 0.3-5Å/Sec, 0.5µm and 1µm

$CdCl_2$: 2%Wt, 450ºC, 10h, N_2

P3HT: 15mg/ml, 1000rpm, 60sec, 150C, 15min

Glod: 45nm

Results and discussion

The IV, QE of devices are plotted in Figure 5-8. Open circuit voltage and short circuit current density for all three devices are listed in Table 5-4.

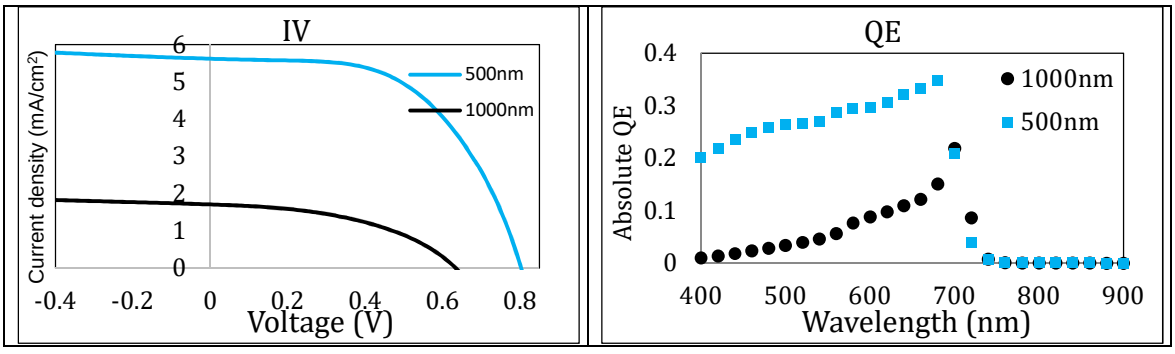


Figure 5-8 IV and QE for NP superstrate devices with two different CdSe thicknesses.

As we explained before in section 5-4, the short circuit current in NP superstrate device is much higher for thinner device compare to thicker device. The current density from QE for 0.5µm device at 450ºC is about 5.65mA/cm^2. IV curve for 0.5µm device shows an excellent voltage about 0.8V that is the highest voltage ever achieved in a solid state CdSe device.

Table 5-4 Open-circuit voltage and current density for NP superstrate with CdS as ETL under different thicknesses. Highest voltage (0.8V) ever achieved in CdSe solar cell.

Device	Thickness (µm)	Voc and Jsc
E6-653	1	0.64V, 1.71mA/cm^2
E6-639	0.5	0.8V, 5.65mA/cm^2

5-4-2-3 Effect of heavily doped ETL

Next we tried to investigate the effect of indium doped CdS as ETL. So here I have two identical samples, one with CdS and another with CdS:In. Both two ETL (30nm) were deposited on FTO substrate at 300ºC followed by a thermal annealing at 400ºC for 30min. CdSe films were deposited at 450ºC on the CdS layer. $CdCl_2$ treatment was done at 450ºC for 10h inside the furnace. The top p-layer was P_3HT and followed by a thick layer of gold contact.

Device structure: FTO/CdS/CdSe/$CdCl_2$/P_3HT/Au

CdS: 200ºC, 100nm, 0.5Å/Sec

CdSe: 450ºC, 0.3-5Å/Sec, 0.5µm and 1µm

$CdCl_2$: 2%Wt, 450ºC, 10h, N_2

P_3HT: 15mg/ml, 1000rpm, 60sec, 150C, 15min

Glod: 45nm

Results and discussion

The IV, QE, and CV of devices are shown in Figure 5-9. Both devices have almost same open circuit voltage (0.8V), but device with CdS:In has higher QE current (7.6mA/cm^2) compare to another. Because CdS:In makes very good ohmic contact with CdSe (see Table 5-5)

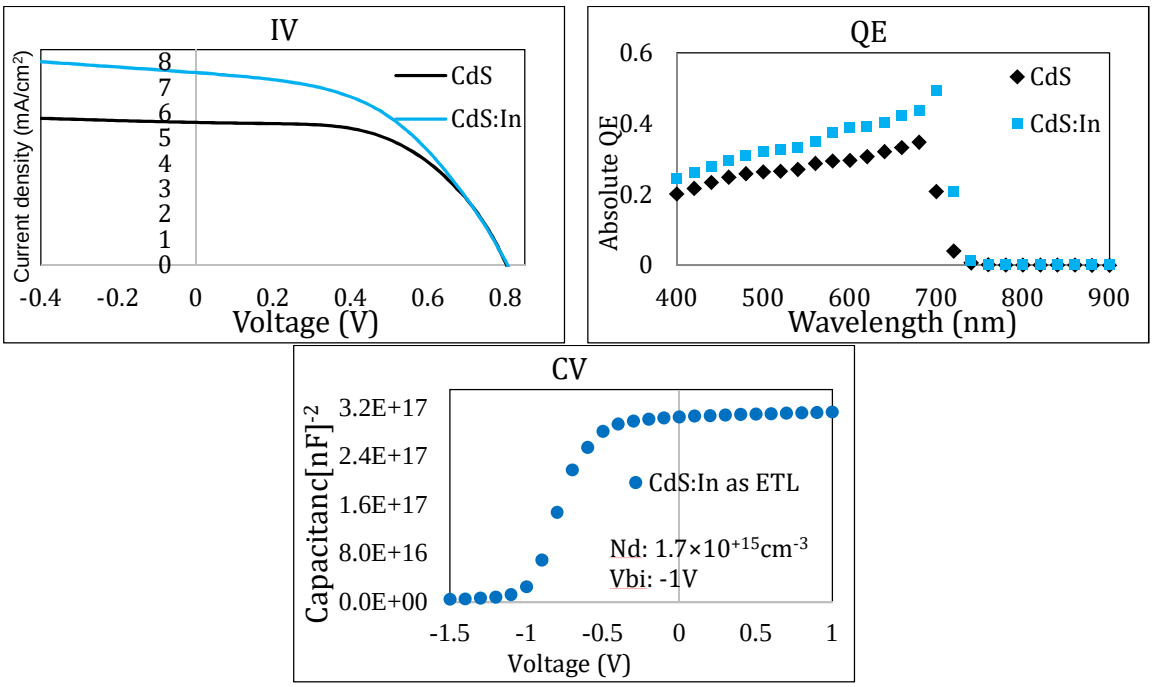


Figure 5-9 IV, QE, and CV for NP superstrate with CdS and CdS:In as ETL.

The standard C-V measurement, shows device has dopant density in the range of 1.7×10^{+15} cm^{-3} and built-in voltage of -1V.

Table 5-5 Open-circuit voltage and current density for NP superstrate with CdS and CdS:In as ETL.

Device	ETL	Voc and Jsc
E6-639A	CdS	0.8V, 5.65mA/cm^2
E6-761L	CdS:In	0.8V, 7.6mA/cm^2

5-4-2-4 Effect of $CdCl_2$ on IV and QE

In this section, we can see the significant effect of $CdCl_2$ heat treatment on device performance. Two identical standard superstrate devices were made. The bulk 0.5µm CdSe layer were deposited at 450ºC. $CdCl_2$ heat treatment was performed at 450ºC for 10h on one device.

Device structure: FTO/CdS/CdSe/$CdCl_2$/P_3HT/Au

CdS: 300ºC, 30nm, 0.5Å/Sec, 400ºC, 30min

CdSe: 450ºC, 0.3-5Å/Sec, 0.5µm

$CdCl_2$: 2%Wt, 450ºC, 10h, N_2

P_3HT: 15mg/ml, 1000rpm, 60sec, 150C, 15min

Glod: 45nm

Results and discussion

As it shown in Figure 5-10, the IV and QE increase significantly upon $CdCl_2$ heat treatment. Open circuit voltage increases from 0.67V to 0.8V that is the highest ever voltage is achieved in this material. Current density also improves about five times from 1.46mA.cm^2 to 7.27mA/cm^2. The exceptional improvement in QE is mainly due to the effect of $CdCl_2$ on grain enhancement and increase in diffusion length of holes as minority light generated carrier.

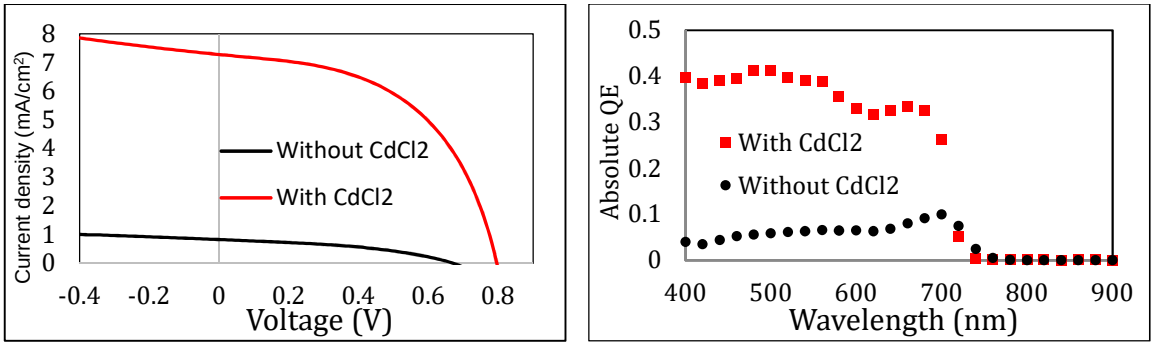


Figure 5-10 IV and QE for NP superstrate devices with and without $CdCl_2$ heat treatment.

Table 5-6 Open-circuit voltage and current density for NP superstrate devices with and without $CdCl_2$ heat treatment.

Device	$CdCl_2$ treatment	Voc and Jsc
E6-734L	NO	0.67V, 1.46mA/cm^2
E6-747L	Yes	0.8V, 7.27mA/cm^2

5-5 PN substrate devices

In next step, we proceeded to work on substrate devices. As we explained in chapter 5-2, for substrate devices light has to come from the top. Developing the wide band gap p-type window organic materials was one the major challenges in this project. We developed PTAA as an organic layer followed by a thin layer of gold (10nm) as top transparent contact. Also we developed a process to deposit indium thin oxide (ITO) top contact on PEDOT:PSS p-layer without damaging PEDOT:PSS. Extra PEDOT:PSS in the area outside of ITO dots was removed using dry air plasma. This technique helps to passivate the remaining PEDOT:PSS and prevents from shorts.

5-5-1 PN substrate device with PTAA/Au on top

We tried to use PTAA as a transparent window organic p-layer. Large bandgap (3eV) of PTAA along with small thickness (~30nm) as a p heterojunction material will assure that most of the incident photons are transmitted and absorbed by CdSe. PN substrate device structure and energy band diagram with PTAA/Au on top, are shown in Figure 5-11.

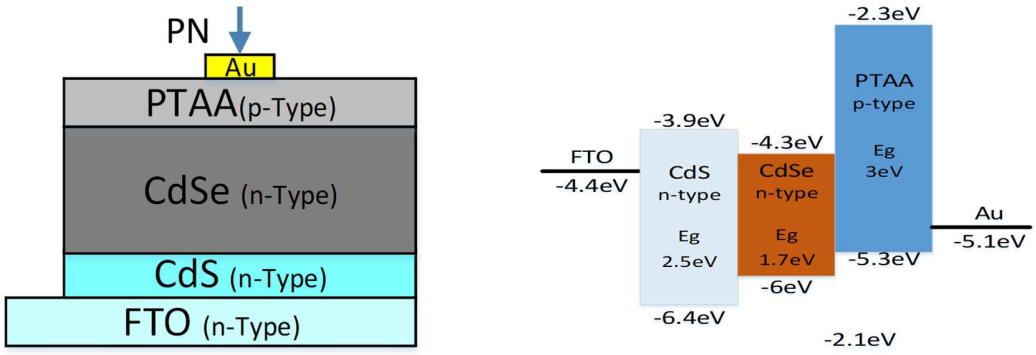


Figure 5-11 Device structure (Left) and energy band diagram (Right) of PN substrate device with PTAA as HTL.

In this experiment 100nm CdS was deposited on FTO substrate at 200ºC substrate temperature as ETL. Then CdSe films (0.5µm and 1µm) were deposited at 400ºC. $CdCl_2$ treatment was

performed at 450ºC on both devices for 10h. The top p-layer was PTAA followed by a thin layer of gold (10nm) contact.

Device structure: FTO/CdS/CdSe/$CdCl_2$/PTAA/Au

CdS: 200ºC, 100nm, 0.5Å/Sec

CdSe: 450ºC, 0.3-5Å/Sec, 0.5µm and 1µm

$CdCl_2$: 2%Wt, 450ºC, 10h, N_2

PTAA: 10mg/ml, 3000rpm, 60sec, 200C, 15min

Glod: 10nm

Results and discussion

The IV and QE of 0.5µm and 1µm devices are plottedin Figure 5-12. Both devices have almost same open circuit voltage (~0.6V), but thicker device has higher QE current (7.69mA/cm^2) compare to thinner device (5.77mA/cm^2).

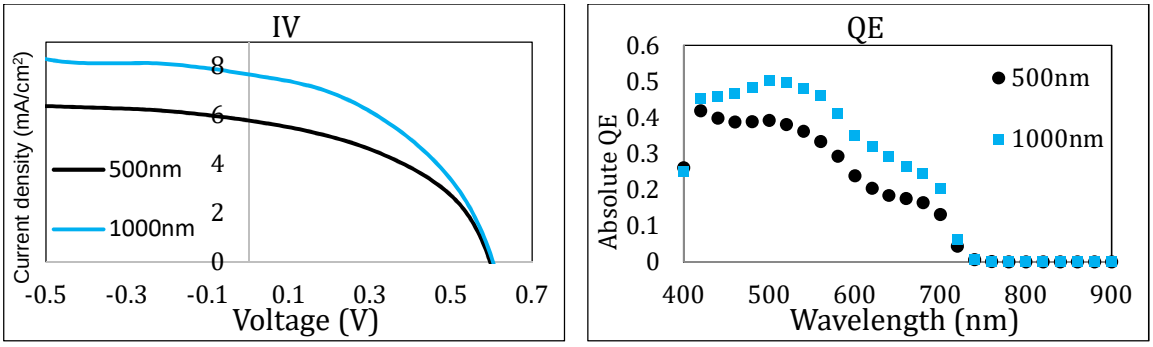


Figure 5-12 IV and QE of PN substrate devices with PTAA as HTL.

Table 5-7 Open-circuit voltage and current density for PN substrate devices with PTAA as HTL.

Device	Thickness (nm)	Voc and Jsc
E6-551	0.5µm	0.6V, 5.77mA/cm^2
E6-543	1µm	0.6V, 7.69mA/cm^2

In PN substrate device, light is coming from p-side. For example, a high energy photon is absorbed in the area close to PN interface and electron-hole will be generated. Holes have to travel into the same distance to be collected in p-side in both thicker and thinner devices. But in substrate device, extra thickness (in thicker device) helps to absorb more photons (low energy) which automatically improves the electron-hole generation probability in bulk CdSe layer (Figure 5-13).

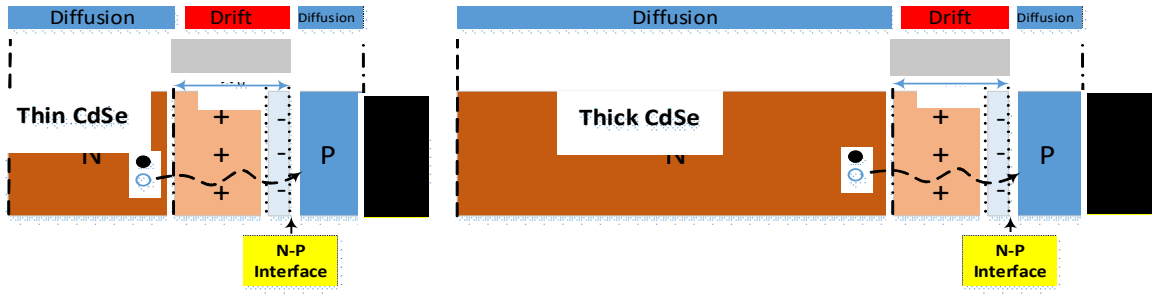


Figure 5-13 The collection of Hole as minority light generated carrier on the p-side in PN substrate device, Thin device (Left) and Thick device (Right).

5-5-2 PN substrate device with PEDOT/ITO on top

We also used PEDOT:PSS as an organic p-layer. Thin layer (30nm) of a large bandgap (3.2eV) HTL will assure that most of the incident photons are transmitted and absorbed by bulk CdSe layer. PN substrate device structure and energy band diagram with PEDOT/ITO on top, are shown in Figure 5-11.

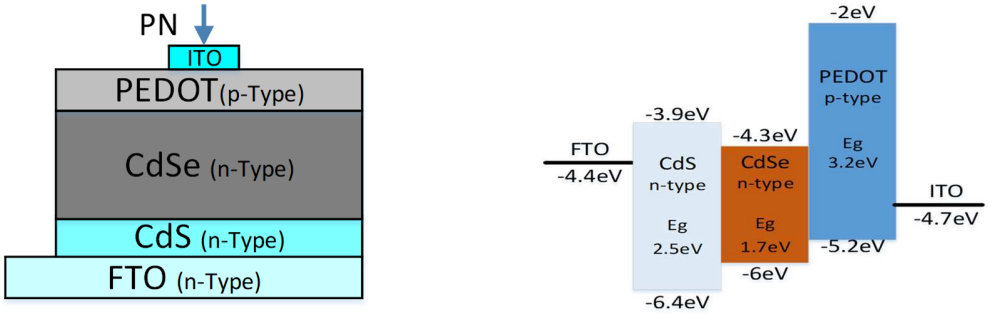


Figure 5-14 Device structure (Left) and energy band diagram (Right) of PN substrate device with PEDOT/ITO on top.

5-5-2-1 Effect of $CdCl_2$ solution concentration

We designed an experiment to optimize the concentration of $CdCl_2$ solution. 100nm CdS was deposited on FTO substrate at 300ºC substrate temperature and annealed at 400ºC for 30min as HTL. Then CdSe film (1µm) was deposited at 450ºC. $CdCl_2$ treatment was done at 500ºC on devices for 10h under three different $CdCl_2$ solution concentration (2%Wt, 4%Wt, and 8%Wt). The top p-layer was PEDOT followed by ITO contacts. 70nm of ITO dots was deposited at 150ºC using sputtering with a 0.1cm^2 mask.

Device structure: FTO/CdS/CdSe/$CdCl_2$/PDEOT/ITO

CdS: 300ºC, 100nm, 0.5Å/Sec, 400ºC, 30min

CdSe: 450ºC, 0.3-5Å/Sec, 1µm

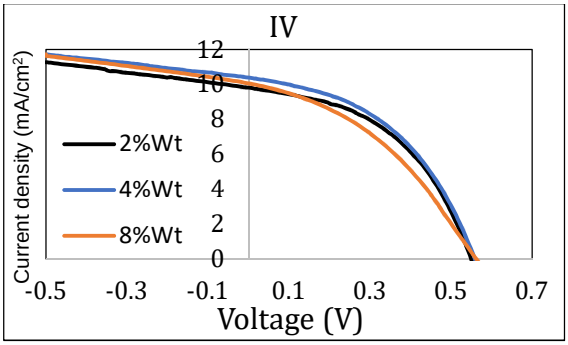
$CdCl_2$: 2%Wt, 4%Wt, 8%Wt, 500ºC, 10h, N_2

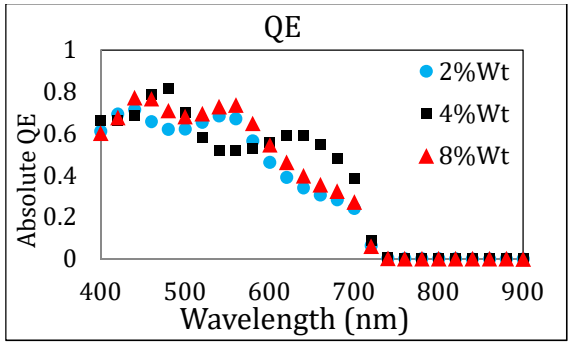
PEDOT: 1000rpm, 40sec, 200C, 15min

ITO: 150C, 70nm, 20W

Results and discussion

The IV, QE, and CV of the devices are shown in Figure 5-12. All three devices have almost same open circuit voltage (~0.6V), but device that used 4%Wt CdCl2 solution gives higher QE current (11.9mA/cm2) compare to other devices (see Figure 5-15 and Table 5-8).





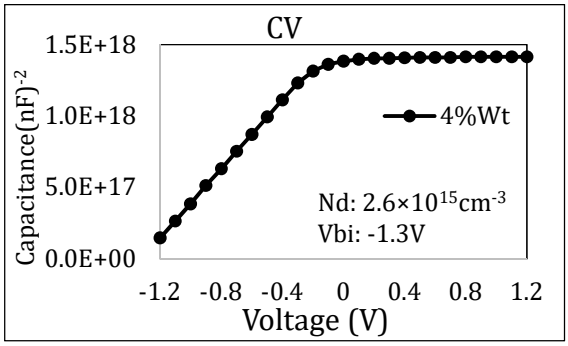


Figure 5-15 (continued) IV, QE, and CV of PN substrate devices with PEDOT:PSS as HTL under different $CdCl_2$ solution concentration.

From the standard CV technique, I have measured dopant density and built-in voltage equal to $2.6\times10^{15}cm^{-3}$ and -1.3V respectively for device under 4%Wt $CdCl_2$ solution concentration (see Figure 5-15).

Table 5-8 Open-circuit voltage and current density for PN substrate devices with PEDOT:PSS as HTL under different $CdCl_2$ solution concentration.

Device	$CdCl_2$	Voc and Jsc
E6-779L	2%Wt	0.6V, 10.69mA/cm^2
E6-780L	4%Wt	0.6V, 11.9mA/cm^2
E6-785R	8%Wt	0.6V, 11.48mA/cm^2

5-5-2-2 Effect of deposition rate

We also optimized the CdSe deposition rate to make efficient heterojunction cell. 100nm CdS was deposited on FTO substrate at 300ºC substrate temperature and annealed at 400ºC for 30min as a ETL. Then 1µm CdSe film was deposited under two different deposition rates (2.5Å/Sec and 5Å/Sec) at 450ºC. $CdCl_2$ treatment was done at 500ºC on devices for 10h under using 4%Wt solution concentration. The top p-layer was PEDOT followed by ITO contacts.

Device structure: FTO/CdS/CdSe/$CdCl_2$/PDEOT/ITO

CdS: 300ºC, 100nm, 0.5Å/Sec, 400ºC, 30min

CdSe: 450ºC, 1µm, 2.5Å/Sec and 5Å/Sec

$CdCl_2$: 4%Wt, 500ºC, 10h, N_2

PEDOT: 1000rpm, 40sec, 200C, 15min

ITO: 150C, 70nm, 20W

Results and discussion

The IV and QE for devices are presented in Figure 5-16. Both devices have almost same open circuit voltage (~0.6V), and device that was deposited under 2.5Å/Sec shows slightly higher QE current (12.51mA/cm^2) (see Figure 5-16 and Table 5-9).

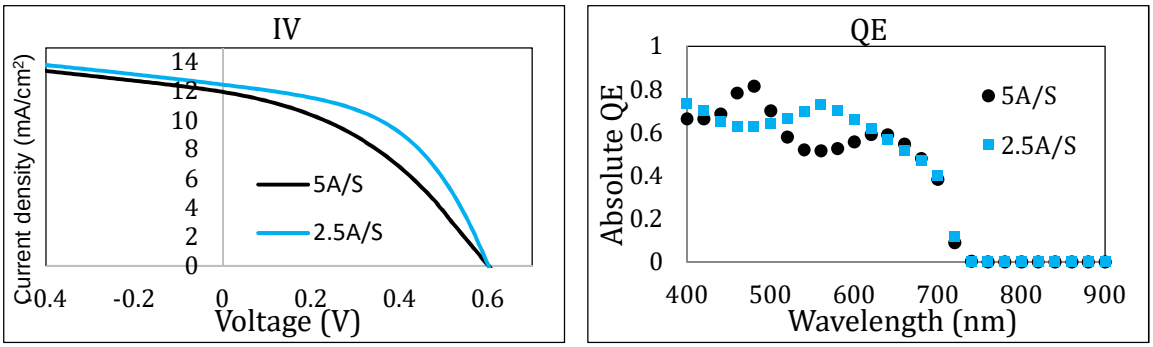


Figure 5-16 IV and QE for PN substrate devices with PEDOT:PSS as HTL under different deposition rate.

Table 5-9 Open-circuit voltage and current density for PN substrate devices with PEDOT:PSS as HTL under different deposition rate.

Device	Rate[Å/S]	Voc and Jsc
E6-780L	5	0.6V, 11.9mA/cm^2
E6-1003R	2.5	0.6V, 12.51mA/cm^2

5-5-3 PN substrate device with p$^+$-a-SiC/ITO on top

This experiment was created with a heavily doped p-type amorphous silicon carbide (p$^+$-a-SiC) as HTL on CdSe layer. A thick layer of CdSe was deposited at 400ºC on n-CdS layer. Because this device is substrate, we decided to make CdSe film about 2µm thick to make sure the film is free of any pinholes which prevents it from shorts. A post-annealing was performed on the device at 400ºC for 10h. PN substrate device structure and energy band diagram are given in Figure 5-17.

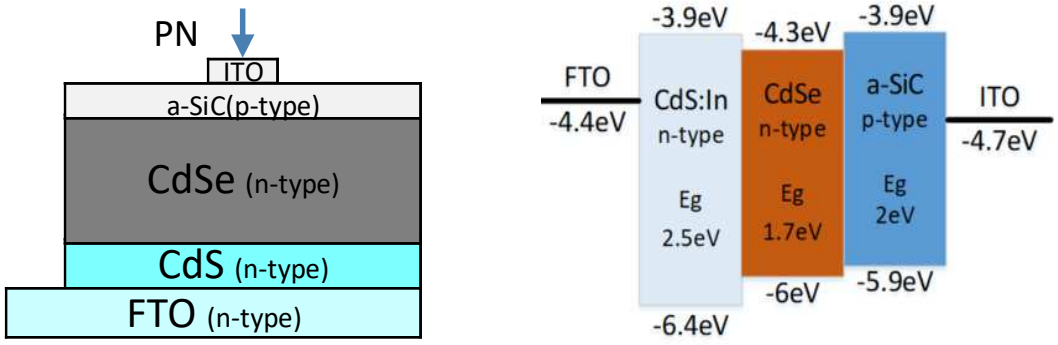


Figure 5-17 Device structure (Left) and energy band diagram (Right) of PN substrate device with p^+-a-SiC /ITO on top.

Device structure: FTO/n-CdS/CdSe/Post-anneal/p^+a-SiC/ITO

n-CdS: 300ºC, 100nm, 0.5Å/Sec, 400ºC, 30min

CdSe: 400ºC, 2µm, 5Å/Sec

Post-anneal: 500ºC, 10h, N_2

p^+-a-SiC: I-layer (15min), p^+-layer

ITO: 150C, 70nm, 20W

Results and discussion

The IV and QE of device are provided in Figure 5-18. It has a decent open circuit voltage equal to ~0.66V, and QE current of 4.2mA/cm^2 (see Figure 5-18 and Table 5-10)

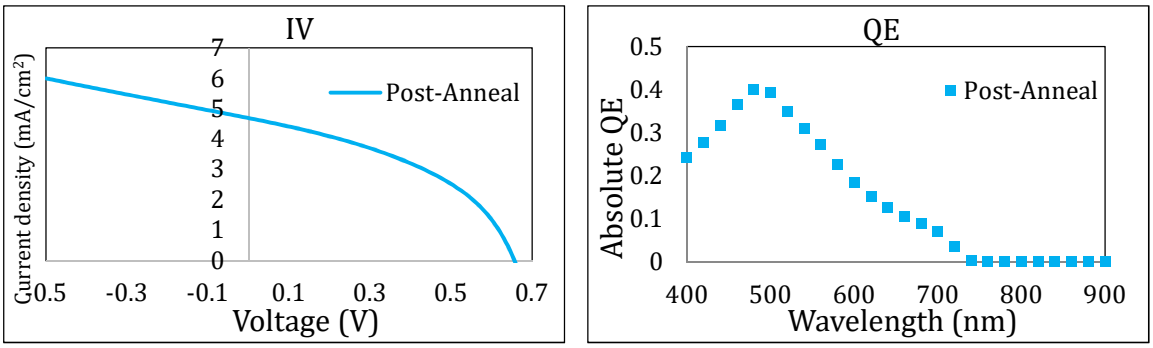


Figure 5-18 IV and QE of PN substrate device with p^+-a-SiC as HTL.

Table 5-10 Open-circuit voltage and current density PN substrate device with p^+-a-SiC as HTL.

Device	Post-Annealing	Voc and Jsc
E6-966R	Anneal: 500C, 10h	0.66V, 4.2mA/cm^2

5-6 NP superstrate and PN substrate devices comparison

In this part, I have done a full device characterization to compare one the best superstrate cell with a best substrate cell. Several fundamental device parameters were measured to compare two cells including Current-voltage (IV), Quantum efficiency (QE), Bandgap ($QE^2 \times Energy^2$ vs. Energy plot), Built-in voltage (V_{bi}) and dopant density (N_d) using Capacitance-Voltgae vs. temperature (CVT), Urbach energy (E_u) from sub-gap QE, Attempt-to-escape frequency (ATEF) using CfT (Capacitance-frequency vs. temperature), Density of state (DOS), Trap energy (E_T), and Dielectric constant of CdSe (ϵ_r). PN substrate and NP superstrate devices structure are shown in Figure 5-19.

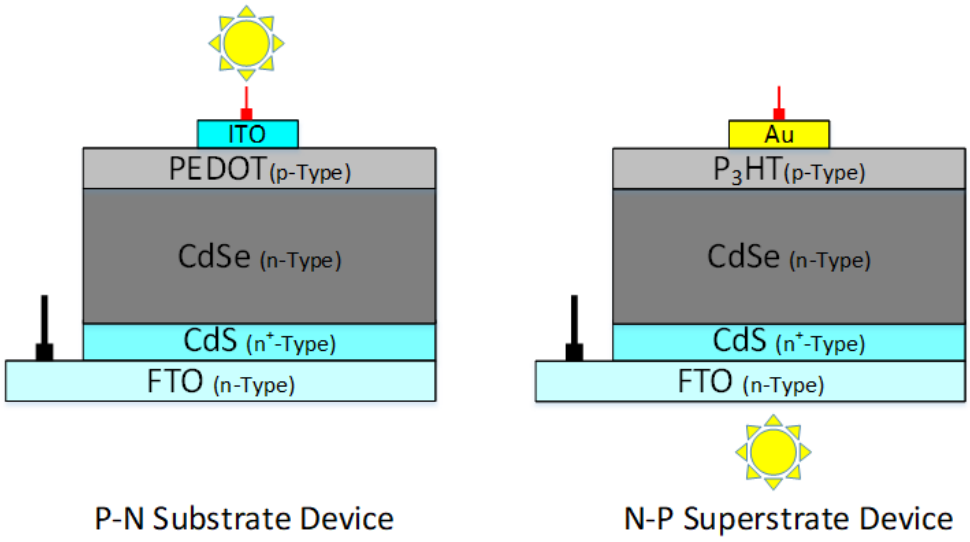


Figure 5-19 PN substrate (Left) and NP superstrate (Right) devices structure.

Superstrate device was prepared by evaporation of 30nm n^+-CdS layer at 300°C on FTO substrate followed by 400°C post-annealing for 30min at air. Then 0.5µm thick CdSe was

deposited at 450ºC and $CdCl_2$ heat treatment was performed at 500ºC for 10h. The top p-layer was P_3HT with a thick layer of gold as top contact.

Device structure (E6-761L): FTO/CdS/CdSe/$CdCl_2$/P_3HT/Au

CdS: 300ºC, 30nm, 0.5Å/Sec, 400ºC, 30min

CdSe: 450ºC, 0.3-5Å/Sec, 0.5µm

$CdCl_2$: 2%Wt, 450ºC, 10h, N_2

P_3HT: 15mg/ml, 1000rpm, 60sec, 150C, 15min

Glod: 45nm

Substrate device was prepared by evaporation of 100nm n^+-CdS layer at 300ºC on FTO substrate followed by 400ºC post-annealing for 30min at air. Then 1µm thick CdSe was deposited at 450ºC and $CdCl_2$ heat treatment was performed at 500ºC for 10h. The top p-layer was PEDOT with ITO as top contact.

Device structure (E6-780L): FTO/CdS/CdSe/$CdCl_2$/PDEOT/ITO

CdS: 300ºC, 100nm, 0.5Å/Sec, 400ºC, 30min

CdSe: 450ºC, 1µm, and 5Å/Sec

$CdCl_2$: 4%Wt, 500ºC, 10h, N_2

PEDOT: 1000rpm, 40sec, 200C, 15min

ITO: 150C, 70nm, 20W

The illuminated I-V and QE curves for both devices are shown in Figure 5-20. Superstrate device has high open-circuit voltage and reasonable current about 0.8V and 7.6mA/cm^2 respectively. But, substrate device has higher current density in the range of 11.9 mA/cm^2 (see Table 5-11).

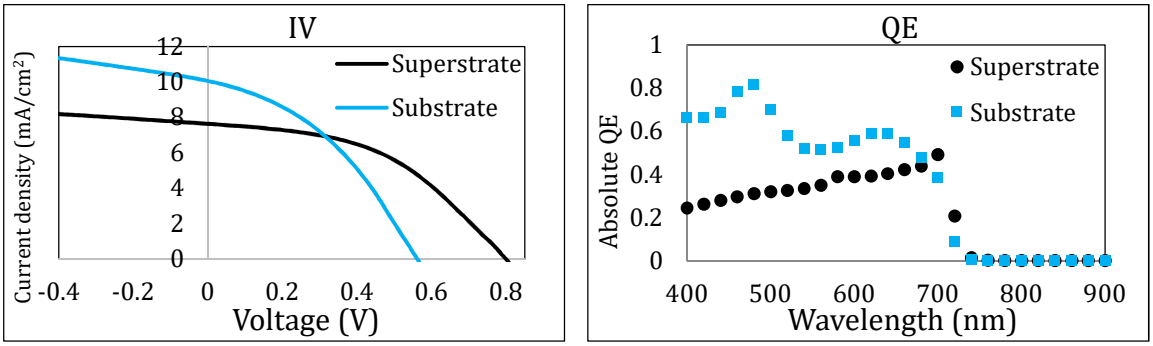


Figure 5-20 I-V and QE for NP superstrate (Black) and PN substrate (Blue) devices.

Table 5-11 Open-circuit voltage and current density superstrate and substrate devices.

Device	Structure	Voc and Jsc
E6-761L	Superstrate	0.8V, 7.6mA/cm^2
E6-780L	Substrate	0.6V, 11.9mA/cm^2

We also calculated bandgap of CdSe device from $(QE \times E)^2$ vs E plot. The intercept of straight line with E axis shows bandgap at 1.7eV. (Where E is photon energy).

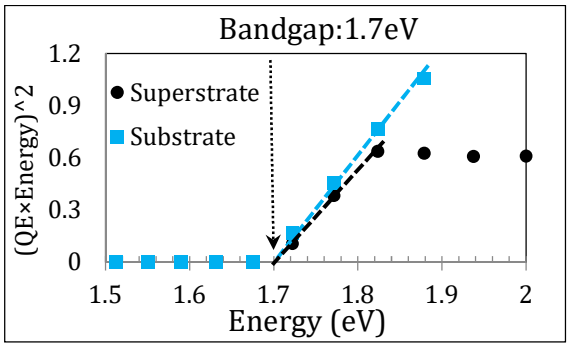


Figure 5-21 $(QE \times E)^2$ vs E for superstrate (Black) and substrate (Blue) devices.

The next experiment was C-V measurement under several different temperature (Chapter 3-6). V-C was measured at room temperature (RT), 50°C, 75°C, 100°C, and 125°C. Capacitance value increases by increasing the temperature. Dopant density and built-in voltage for superstrate device at RT are 2.45×10^{15} cm^{-3} and -1V respectively. Dopant density and built-in voltage for substrate device at RT are 2.6×10^{15} cm^{-3} and -3V respectively.

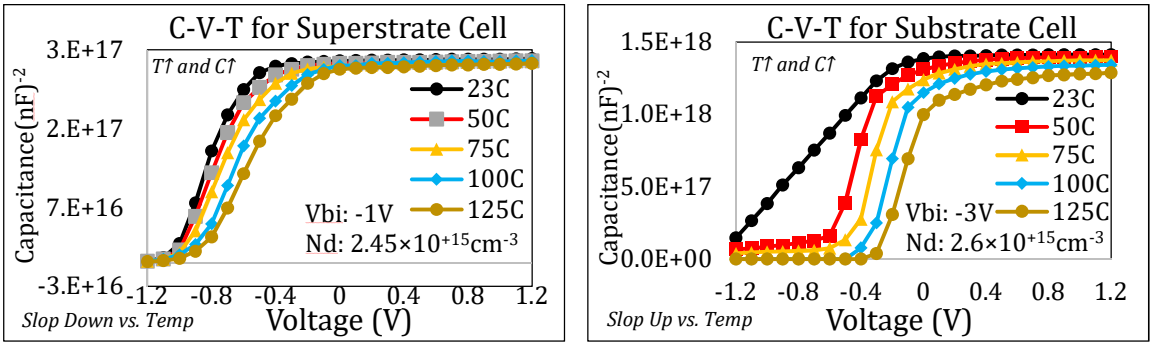


Figure 5-22 C-V vs temparature for NP superstrate (Left) and PN substrate (Right) devices.

We measured Urbach energies of tail states and mid-gap defects using Sub-gap QE for both superstrate and substrate devices.

Basically, n type semiconductor has tail states near the valence (Red) and conduction bands. Also it has mid-gap defects in the middle of the bandgap (Green). Photon with energies below the bandgap excite electrons from the valence to the conduction band and create holes behinds. We found Urbach energy of 15.6meV for the valence band edge. Lower value of Urbach energy shows the semiconductor material is less defective.

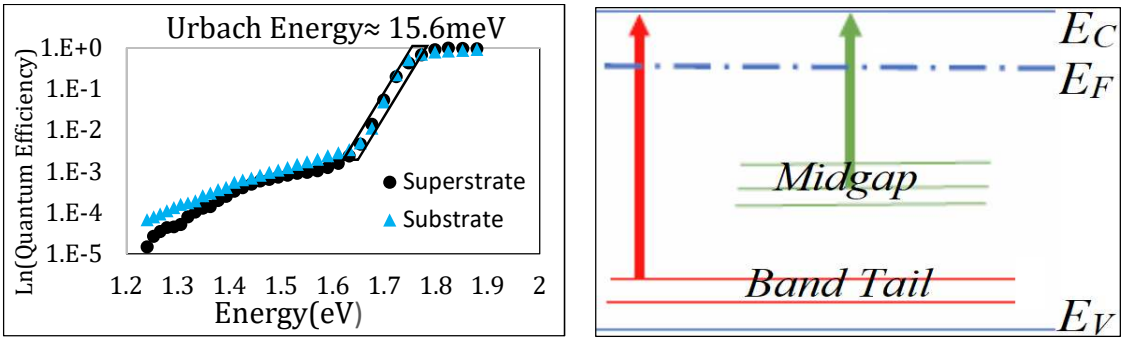


Figure 5-23 Sub-gap QE vs energy for NP superstrate (Black) and PN substrate (Blue) devices.

The CfT experiment was performed to measure mid-gap defects (Chapter 3-7). As we explained before, capacitance was measured by varying frequency at different temperature (see Figure 5-24). Shallow trap has fast emission rate and deep trap has slow emission rate. All the traps (Shallow and deep) response and contribute to the measurement at low frequency, so

capacitance value is comparatively high. But under high frequency only shallow traps can response and contribute to the measurement, so capacitance value deceases. So capacitance decreases by increasing the frequency.

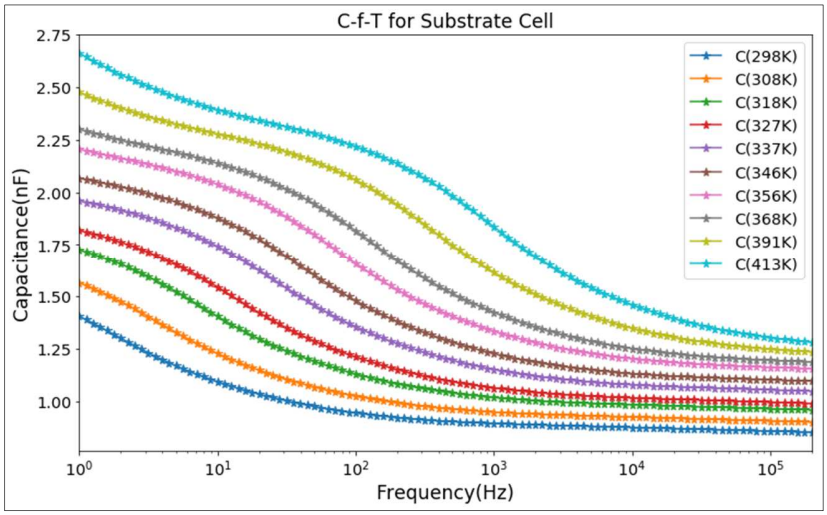


Figure 5-24 C-f-T for PN substrate device under different temperature.

The peaks in –f dC/df vs. frequency curves at different temperatures are correspond to ATEF.

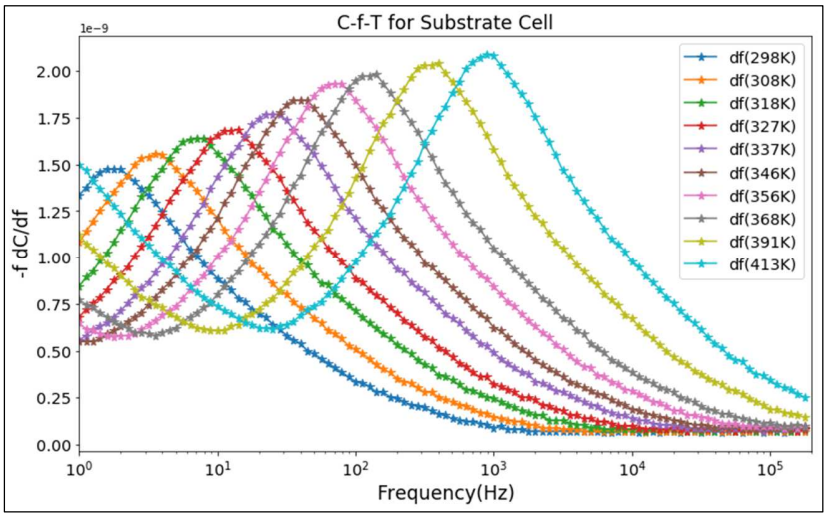


Figure 5-25 –f dC/df for PN substrate device under different temperature.

These peaks are corresponds to the activation energy of the traps. So the slop and intercept of arrhenius plot, Ln(fpeak) vs. (1/kT) are coresponding to activation energy and ATSF

respectively (see Figure 5-26). The primary data indicates a deep trap energy of 0.52eV bellow the conduction band. ATSF and relative dilectric constant (ϵ_r) are measured 2×10^9Hz and 10.4 respectively.

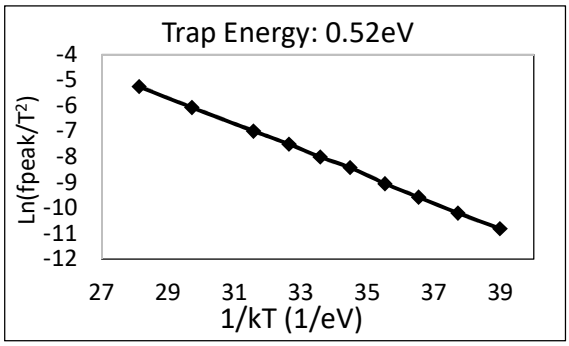


Figure 5-26 Determination of activation energy for the deep trap in CdSe using Arrhenius curves of peak frequencies.

Capacitance vs frequency at room temperature for superstrate and substrate devices are shown in Figure 5-27 (Left). Defect density vs. energy for CdSe device Figure 5-27 (Right) indicates shallow trap energy at 0.24eV and deep trap energy at 0.53eV that is in good agreement with activation energy shown in Figure 5-26.

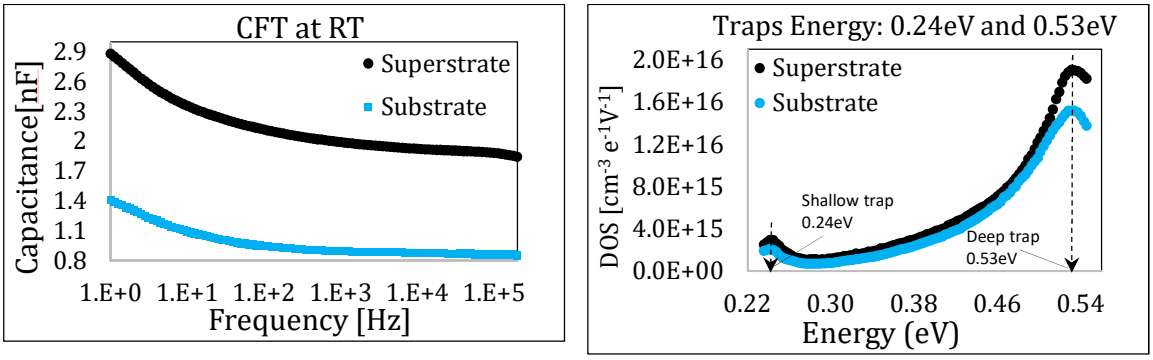


Figure 5-27 Capacitance vs frequency at room temprature for superstrate (Left-Black) and substrate (Left-Blue) devices. Defect density vs. energy for a CdSe device (Right).

CHAPTER 6. CONCLUSIONS

In this work, I have explored the fundamental electronic and optical properties of CdSe material for photovoltaic application.

First of all, a new thermal evaporation system (E6-TE), single zone quartz tube cadmium chloride furnace and two zone quartz tube post-selenization furnace were designed and made for this project to make uniform, high quality, and reproducible CdSe films.

We have deposited CdSe thin film using thermal evaporation on different substrate at high substrate temperature (300-450^{o}C) and we achieved uniform CdSe thin film.

Optical data including, transmission, reflection, and absorption spectrums showed the CdSe is about 80% transparent from 720nm to 2500nm while significant absorbance from 400nm to 720nm. The absorption coefficient (α) vs. energy (E) graph shows CdSe has high $\alpha \approx 9\times10^{4}cm^{-1}$ for higher energy photons range. Also, we calculated a direct optical bandgap of ~1.72eV by extrapolating the straight line on the energy axis.

The grain size of as-deposited CdSe is around 0.3um. We developed cadmium chloride treatment process for CdSe thin film. This process has a significant effect to improve the grain sizes up to 2µm for CdSe film on FTO/CdS substrate. In addition, the largest grain enhancement (~27X larger) was achieved up to 8µm on glass for CdSe with Se flux. The SEM images shown that the grain sizes increase by increasing the film thicknesses. The SEM cross section images confirms that $CdCl_2$ penetrates perfectly into the depth of 0.5µm.

We developed post-deposition selenization process on CdSe thin film. This process significantly improved the grain sizes up to 5.7µm. Selenization improved the photo-conductivity from $2.94\times10^{-4}\,(\Omega.cm)^{-1}$ to $1.2\times10^{-3}\,(\Omega.cm)^{-1}$ for as-deposited and 2 hours post-selenized samples respectively (~36 times larger). Also it increased the light-to-dark

conductivity ratio from 79 to 1.2×10^{6} for as-deposited and 2 hours post-selenized samples respectively (~1.5×10^{4} times larger).

The electron mobility-lifetime product was another important electronic parameters that increased significantly under post-selenization. This product from photoconductivity was measured about 5.6×10^{-6} cm^2/V.

SCLC technique was used to measure mobility of CdSe films. Systematic study was performed to increase electron mobility up to $3.5cm^2/V.s$ using SCLC technique.

The sub-bandgap photo-conductivity vs. photon energy measurement was performed to find tail states near the conduction and valence bands. We showed the deduced density of tail states as a function of photon energy (E) for three films, without grain enhancement, with grain enhancement, and with post-selenization. The Urbach energy of valence band tails for the best film under post-selenization was 21meV.

We performed EDS technique to analysis the chemical composition of CdSe thin films. We discovered that, one of the key steps to perform accurate EDS analysis, is applying high enough acceleration voltage about 20KeV. Se to Cd ratio of CdSe thin films under 20KeV using Se K line for different samples including with and without $CdCl_2$ and selenium flux is almost close to one.

In the next step, we designed the efficient heterojunction CdSe solar cell. In this design, the n-layer can be n-CdS or n-TiO_2 and p-layers can be either organic p-layers such as PTAA, P_3HT, PEDOT:PSS or inorganic layers such as p-a-(Si,C) or Cu doped ZnTe.

We developed new NP superstrate device structure with FTO/CdS on bottom and P_3HT/Gold on the top which leds to significant high voltage. Cadmium chloride thermal

activation process was used to passivate the recombination centers. Device with $CdCl_2$ treatment showed much higher current compare to device without $CdCl_2$.

The highest Voc (world record) ever achieved in CdSe solar cells (0.8V) and current density 8mA/cm^2.

Dopant density and build-in voltage were measured 1.7×10^{15} cm^{-3} and -1V respectively. We discovered that only 1-2µm CdSe film is needed to absorb the all photons. Also 2µm grains were achieved under $CdCl_2$ treatment (at 500C for 10h).

In addition, we developed new substrate device structure with FTO/CdS on bottom and PEDOT:PSS /ITO on top which led to significant high current. Voltage and current density for substrate devices were achieved 0.62V and 12mA/cm^2 respectively. The optimum deposition rate and $CdCl_2$ concentration for best device were achieved under 2Å/S and 4%Wt respectively.

Moreover, I performed a systematic study to characterize and compare two superstrate and substrate cells. Among the fundamental device parameters, the superstrate device shown higher voltage (0.8V) compare to substrate device (0.6V). On the other hand, substrate device gave higher current density (11.9mA/cm^2) compare to superstrate device (7.6mA/cm^2). Dopant density, optical bandgap, urbach energy, shallow trap and deep trap energy, for both device are almost identical around 2.5×10^{15} cm^{-3}, 1.7eV, 15.6meV, 0.24eV and 0.53eV below conduction band respectively. Attempt-to-escape frequency and relative dilectric constant (ϵ_r) were measured 2×10^9Hz and 10.4 respectively.

APPENDIX A. EFFICIENT HETEROJUNCTION THIN FILM CDSE SOLAR CELLS DEPOSITED USING THERMAL EVAPORATION

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Behrang Bagheri, Ranjith Kottokkaran, Laila-Parvin Poly, Saba Sharikadze, Ben Reichert, Max Noack and, Vikram Dalal.

Iowa State University, Microelectronics Research Center, Ames, Iowa, USA

Abstract — CdSe is potentially an important material for making tandem junction solar cells with Si and CIGS. Thermodynamic calculations reveal the potential ShockleyQueisser efficiency of such a tandem cell to be in the 45% range. CdSe has the optimum bandgap (1.72eV) for a tandem cell with Si. In this paper, we show that this material system is indeed capable of achieving good electronic properties and reasonable devices can be made in the material. We report on fabricating CdSe materials and heterojunction CdSe solar cells in both superstrate and substrate configurations on FTO/glass and metal substrates. CdSe layer was deposited using thermal evaporation and then was post-treated with CdCl2 to enhance the grainsize and passivate grain boundaries. The device was an ideal heterojunction structure consisting of glass/FTO/n^+CdS/nCdSe/p-organic layer/N_iO/ITO. The n^+CdS layer acted to prevent hole recombination at the n^+/n interface, and the p-organic layer (such as PEDOT:PSS or P_3HT) acted to prevent electron recombination at the p^+/n interface. The N_iO layer was deposited on top of the organic layer to prevent decomposition of the organic layer during ITO deposition. World-record opencircuit voltages exceeding 800mV and currents of ~15 mA/cm^2 were obtained in devices. Detailed material measurements such as SEM revealed large grain sizes approaching 8 micrometer in some of the films after grain enhancement. Optical measurements and QE measurements show the bandgap to be 1.72 eV. XPS measurements

showed the CdSe film to be n type. Space-charge limited current was used to measure electron mobilities which were in the range of 1-2 cm^2/V-s. Capacitance spectroscopy showed the doping densities to be in the range of a few x $10^{15}/cm^3$. For substrate devices, the quantum efficiency obtained was in the 90% range.

I. Introduction

Photovoltaic energy conversion is now a major energy technology. Si technology dominates the PV production today, with the conversion efficiencies of commercial products reaching 20+%, and of laboratory cells reaching 26+%. Since balance of system costs dominate the overall cost of PV energy, a technology for increasing the efficiency of Si panels by 50% would lead to significant reduction in the cost of PV energy. In this paper, we investigate a thin film material system (CdSe), which in a tandem junction combination with Si, can achieve such a large increase in the efficiency of Si based panels. CdSe is a direct gap material with the right bandgap (~1.72eV) to match with Si in a tandem cell configuration. In Fig. 1 we show the projected ShockleyQueisser efficiency of a CdSe/Si system, showing that efficiencies approaching 45% are possible [1]. This means that actual production efficiencies of 35-38% should be possible for PV panels based on such a technology. In spite of the enormous potential of this material system, there is little work on PV devices in this material [2-5]. In this paper, we present the first ever systematic study of structure, electronic properties and device properties of this material, including using a novel heterojunction structure to optimize QE and chemical annealing techniques to improve the grain size and reduce grain boundary recombination.

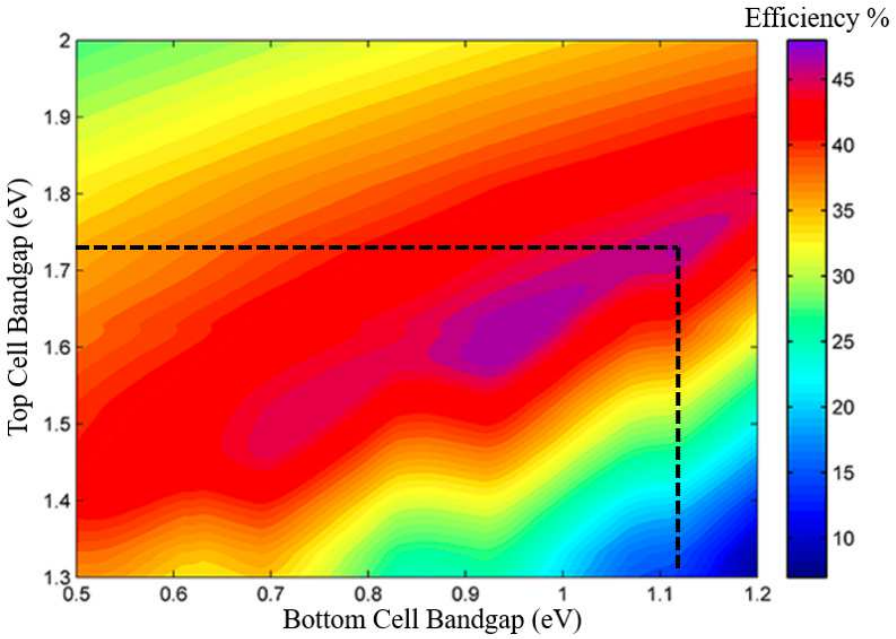


Fig.1 Projected thermodynamic PV efficiencies in a tandem cell as a function of top cell bandgap (vertical axis) and bottom cell bandgap (horizontal axis). CdSe has the right bandgap (~1.72eV) for the top cell and Si has the right bandgap (1.12eV) as the bottom cell for achieving ~45% SQ efficiency [1].

II. Properties of CdSe

CdSe is a direct gap material. In Fig. 2 we show the absorption data on one of our CdSe films showing a bandgap of 1.72eV. The film was deposited using thermal evaporation from CdSe chunks using a Luxel furnace. Typical substrate temperatures during growth were in the range of 400- 500°C. We discovered that the grain size can be significantly increased by using a post-deposition $CdCl_2$ heat treatment at 450°C. See Fig. 3 for SEM data on grain enhancement. XPS measurements showed that the film was n-type with the valence band being 1.2eV below the Fermi level. Electron mobility was measured using space charge limited current techniques and was found to be in the range of 3.5cm^2/V-s.

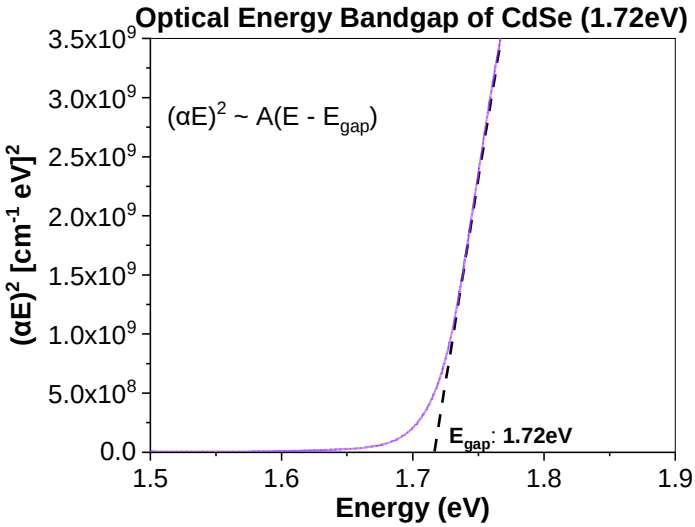


Fig. 2 $(\alpha.E)^2$ vs. E curve showing intercept at ~1.72 eV

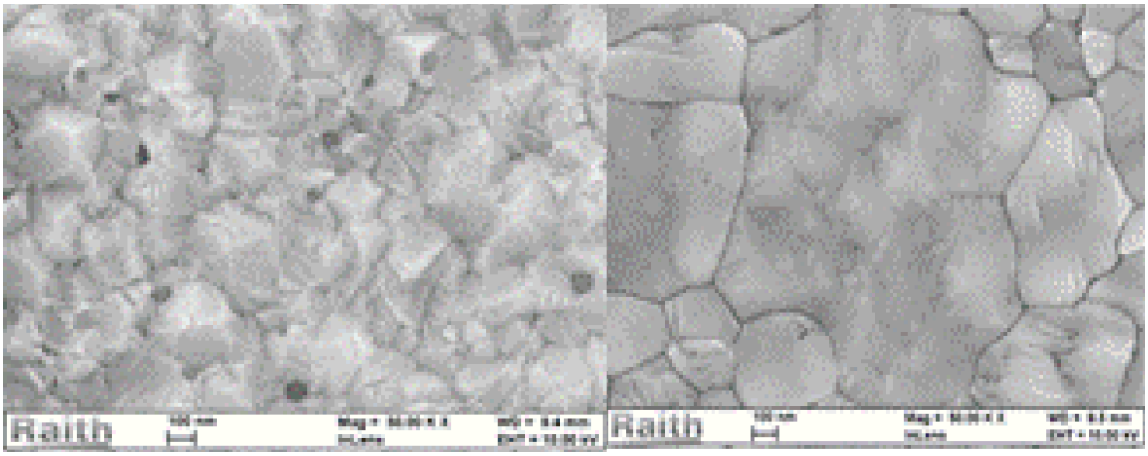
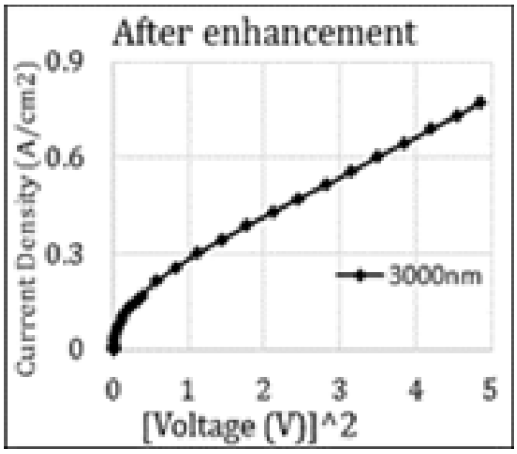


Fig. 3 SEM of grains before (left) and after (right) $CdCl_2$ treatment for samples deposited on FTO/glass.

Drift motilities were measured using space-charge limited current techniques [6] in both annealed and un-annealed films. The results are shown in Fig.4 and 5 below.



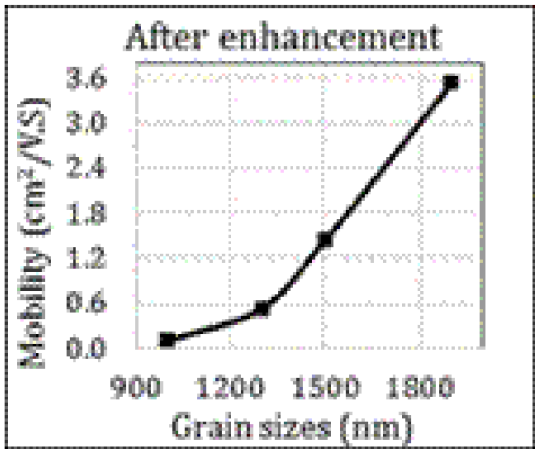


Fig.4 (Left) Current vs. Voltage relationship for CdSe films.

Fig. 5 (Right) Mobility vs. grain size after $CdCl_2$ treatment.

III. Device structure

Heterojunction devices were made by using n^+CdS as the n heterojunction layer and an organic semiconductor as p-layer. Three different organic semiconductors were used: P_3HT, PTAA and PEDOT:PSS. The reason for using these heterojunction layers was to provide the optimum heterojunction to prevent recombination at the p-n and n^+-n interfaces. For superstrate devices, we used FTO coated glass and for substrate devices, we used either FTO/glass or aetal. See Fig. 6 for the basic device structure and Fig. 7 for the band diagram of the heterojunction.

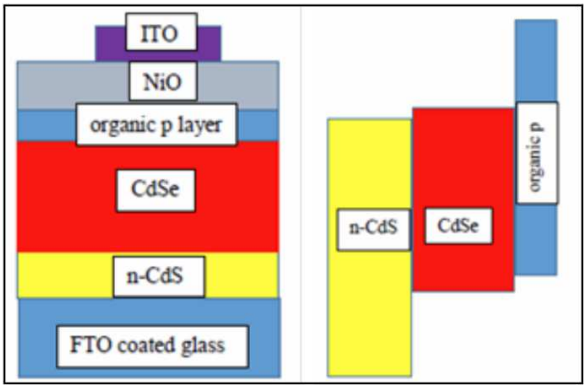


Fig. 6 (Left) Heterojunction Device structurefor a substrate device

Fig. 7 (Right) Band alignments for the n^+CdS-n CdSe and p-organic layers

IV. Device results and influence of post-deposition annealing

A major discovery we made was that the performance of the devices could be improved significantly upon annealing the CdSe films after deposition using a $CdCl_2$ heat treatment. A thin film of $CdCl_2$ solution in water was deposited on the film after growth and annealed in a nitrogen atmosphere at various temperatures. It was found that the optimum anneal temperature was 450°C. The film was annealed for 10hours. Higher temperatures anneals led to loss of Se and poorer device performance. In Fig. 8 we show the I-V curve for a superstrate n+/n/p device with light from the n+side. This is obviously the wrong direction for light- for an optimum device it should be entering from the p side; this structure was used to optimize the grain enhancement and Chlorine passivation technique. Note how the current increases significantly upon annealing.

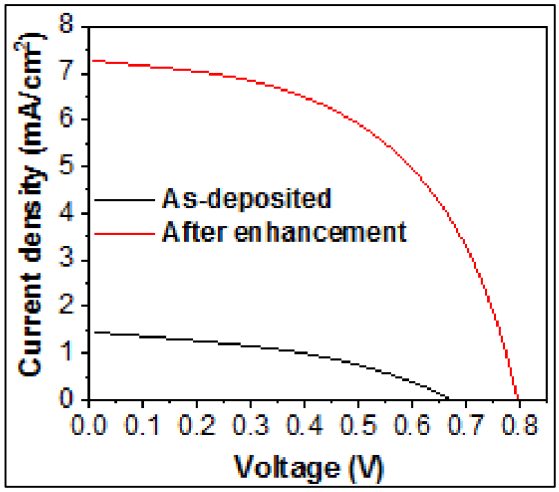


Fig. 8 I-V curve for a superstrate n+/n/p device with light incident from the n^+side. Note how the curve improves significantly upon chemical annealing with $CdCl^2$. The open circuit voltage achieved is the highest ever in this material.

In Fig.9 we show the influence of the grain enhancement technique on quantum efficiency- notice the exceptional increase in QE upon grain enhancement, indicating a significant increase in diffusion length of holes.

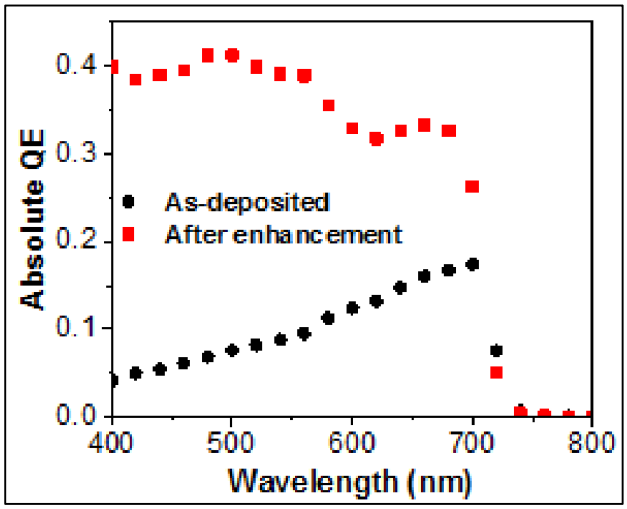


Fig. 9 Influence of $CdCl^2$ treatment on quantum efficiency of superstrate devices with light incident from bottom n-side. Note the significant increase in QE upon $CdCl_2$ treatment, particularly for short wavelength photons which are absorbed far away from the p-n junctions. This fact indicates that the diffusion length of holes has increased significantly upon $CdCl_2$ treatment.

We next proceeded to make substrate devices (light coming from the top). To do this, we had to develop a process for depositing ITO on top of an organic material (PTAA or PEDOT:PSS). We discovered that one could directly deposit ITO on top of PEDOT:PSS without damaging PEDOT:PSS. After the deposition of ITO dots, one had to do dry air plasma passivation of the remaining PEDOT to prevent it from degrading due to moisture and causing shorts. In Fig.10, we show I-V curve of one of the substrate devices showing an excellent current (~10 mA/cm^2) and a decent voltage (056V), much higher than the previously reported 0.2-0.3V [3]. We need to significantly reduce the shunt conductance in substrate devices to improve the performance.

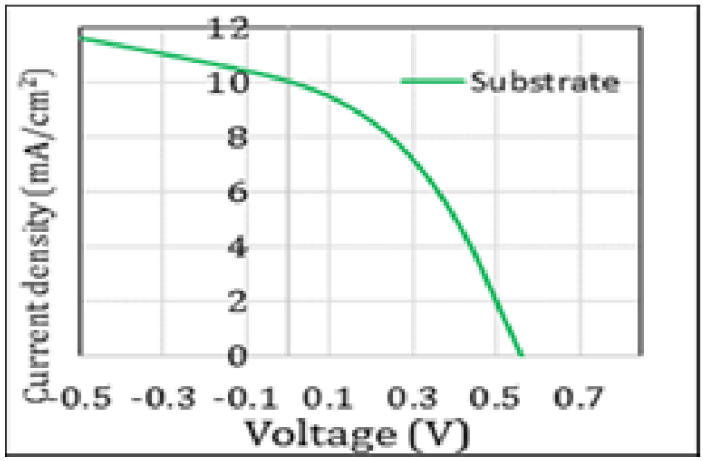


Fig. 10 I-V curve of a substrate device in CdSe, with a top ITO contact on top of the organic heterojunction p layer. Light is incident from the top. Note the excellent current (>10 mA/cm_2) and reasonable open-circuit voltage, 0.56V.

V. Conclusions

In summary, we have shown how one can significantly improve the photovoltaic properties of CdSe solar cells by using post-deposition annealing using a $CdCl_2$ over layer at temperatures of 450°C. Such annealing increases the grain size, the drift mobility and also significantly improves quantum efficiency in devices. We also show that by using appropriate heterojunctions, including the use of inorganic n+CdS as the n type layer and organic layers (P3HT, PTAA, PEDOT:PSS etc.) as a p-type heterojunction layers. We made both substrate and superstrate type of cells, with light coming either from the top or bottom. A worldrecord 0.8V of open circuit voltage was achieved in superstrate cell. We have solved the problem of depositing a transparent contact on top of the organic layer by using an appropriate organic heterojunction layer (PEDOT:PSS) and following it with ITO deposition, which is followed by plasma annealing in a dry air plasma to reduce shunt and to passivate PEDOT.

VI. Acknowledgments

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APPENDIX B. INFLUENCE OF POST-DEPOSITION SELENIZATION AND CADMIUM CHLORIDE ASSISTED GRAIN ENHANCEMENT ON ELECTRONIC PROPERTIES OF CADMIUM SELENIDE THIN FILMS

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Authors: Behrang Bagheri,[1,2] Ranjith Kottokkaran,[2] Laila- Parvin Poly,[1,2] Ben Reichert,[1,2] Saba Sharikadze,[1,2] Max Noack[2] and Vikram Dalal[1,2,a)]

Affiliations

[1]Department of Electrical and Computer Engineering, Iowa State University, Ames, Iowa 50011, USA

[2]Microelectronics Research Center, Iowa State University, Ames, Iowa 50011, USA

[a)]Author to whom correspondence should be addressed: vdalal@iastate.edu

Keywords: Cadmium selenide, Cadmium chloride, Post-selenization, Thermal evaporation, Mobility, Photoconductivity, Scan electron microscopy.

Abstract

We report on the growth, grain enhancement, doping and electron mobility of Cadmium Selenide (CdSe) thin films deposited using thermal evaporation method. The optical measurement shows CdSe is a direct bandgap material with optical bandgap (E_{gap}) of 1.72eV. CdSe thin films were deposited on fluorine doped thin oxide (FTO) glass substrate at different thicknesses, and grain size and mobility were measured on the films. $CdCl_2$ was deposited on the films, and the films were subjected to high temperature treatment for several hours. It was found that both the grain size increased significantly after $CdCl_2$ treatment. Mobility of electrons was measured using the space charge limited current technique and it was found that the mobility increased significantly after $CdCl_2$ treatment. It was discovered that post-deposition selenization further improved the electrical properties of CdSe thin films by increasing the electron mobility-lifetime product and the photo/dark conductivity ratio. CdSe films after post-selenization showed also showed significantly lower values for midgap states and Urbach energies of valence band tail states.

I. Introduction

CdSe is an II-VI group semiconductor chalcogenide which is potentially an attractive material for photovoltaic energy conversion since its bandgap is in the range (~1.7 eV) needed for use in a tandem junction solar cell with Silicon acting as the bottom cell[1-3]. Theoretical calculations

indicate that it is possible to attain a thermodynamic efficiency of ~45% in a tandem cell of CdSe and c-Si[4]. CdSe is a binary compound and as such stoichiometry is easier to achieve than in a ternary or quaternary material. CdSe is not water soluble and does not thermally decompose, unlike Pb-halide pervoskites[5]. It is a direct bandgap semiconductor[6,7] and consequently, only a thin film is needed to absorb photons. CdSe thin films can be deposited using different techniques including thermal evaporation[2], close-spaced sublimation[8], and sputtering[9]. In this work, we report on deposition using physical vapor deposition at high growth temperature of ~400°C with different thicknesses in the range of 0.5µm to 3µm. We show that post-deposition treatments using $CdCl_2$ increases the grain size and mobility of the CdSe significantly. Further high temperature selenization treatment under a Se flux serves to increase the mobility still more.

II. Experimental procedure

For optical characterization, a glass/CdSe structure was prepared using thermal evaporation at a working pressure of 3×10^{-6} Torr. Luxel Radak furnaces with excellent temperature control were used to deposit the films. Two Radak furnaces could be used to deposit CdSe and Se simultaneously. Typical film thicknesses were in the range of 0.5-3µm. For morphological and electrical characterization, films were deposited on various substrates, including glass, Fluorinated tin oxide[10] (FTO), FTO coated with n-CdS and Si wafers. Next, $CdCl_2$ treatment was carried out on some of the samples. The $CdCl_2$ treatment consisted of spin coating of 2%wt. solution of $CdCl_2$ in deionized (DI) water (2g/100mL), followed by thermal annealing under nitrogen atmosphere at 450ºC for 30min inside a quartz tube. For photoconductivity experiment, after CdSe evaporation, post-selenization step was performed at 450ºC on three samples for 30min, 60min and 120min under nitrogen flow inside the quartz tube. The optical properties were measured using Cary 5000 UV-Vis-NIR spectrophotometer in 400–2500nm wavelength range.

III. Results and discussion

A. Optical properties

Optical absorption data, absorption coefficient α vs. E, where E is photon energy, of 1um CdSe film deposited at 400ºC on glass substrate is shown in Fig. 1(a). The plot of $(\alpha.E)^2$ vs. E is shown in Fig. 1(b). It shows a linear dependence with an intercept at 1.72eV, implying a bandgap of 1.72eV.

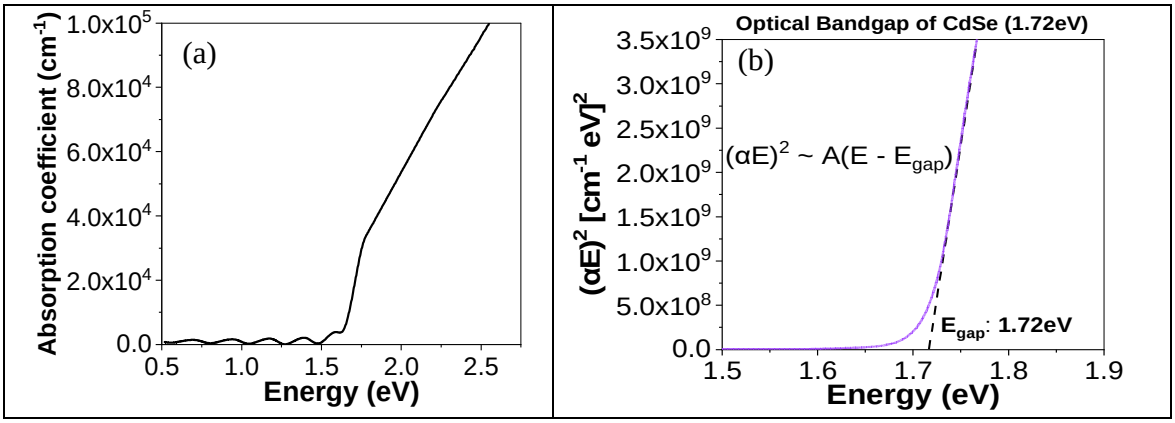

Fig. 1 Optical data of CdSe film, (a) Plot of α vs. E, (b) Plot $(\alpha E)^2$ vs. E.

B. Surface morphological analysis under grain enhancement

The surface morphology of the various CdSe films were assessed using a SEM. See Fig. 2. $CdCl_2$ heat treatment was found to have a significant impact on the grain size, achieving grain enhancement as shown in Fig. 3. The grain sizes after grain enhancement are about 1µm, 1.3µm, 1.5µm, and 1.9µm for the films whose thicknesses were 0.5µm, 1µm, 2µm, and 3µm respectively. SEM images clearly show that films surface become flat and smooth after the $CdCl_2$ treatment.

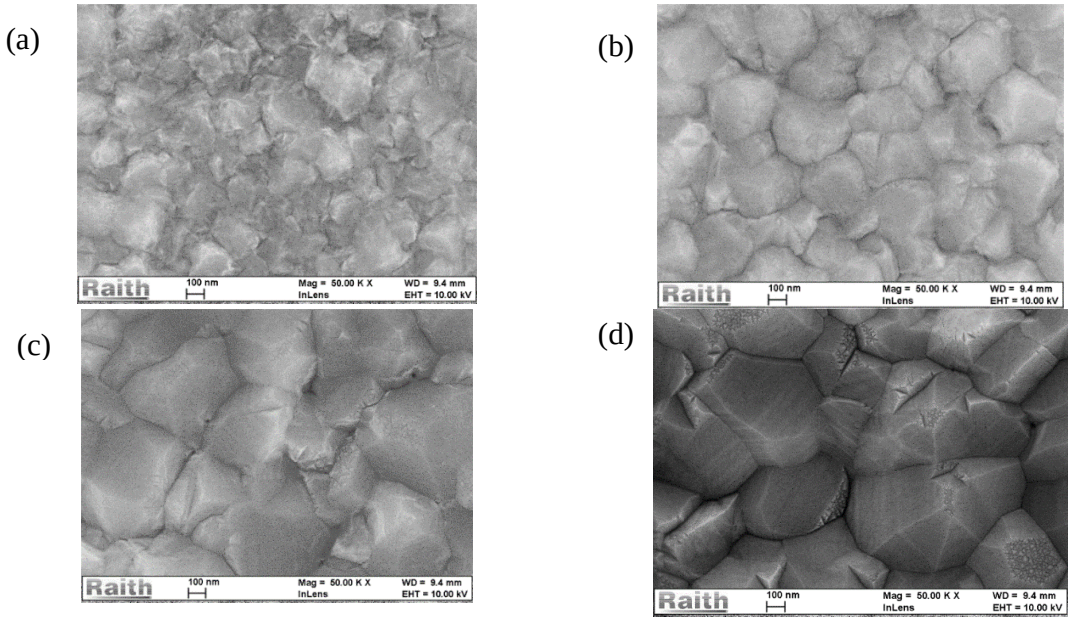

Fig. 2 SEM images of as-deposited CdSe thin films, (a) t: 0.5µm, GS ~0.3µm, (b) t: 1µm, GS ~0.5µm, (c) t: 2µm, GS ~0.7µm, (d) t: 3µm, GS ~0.9µm.

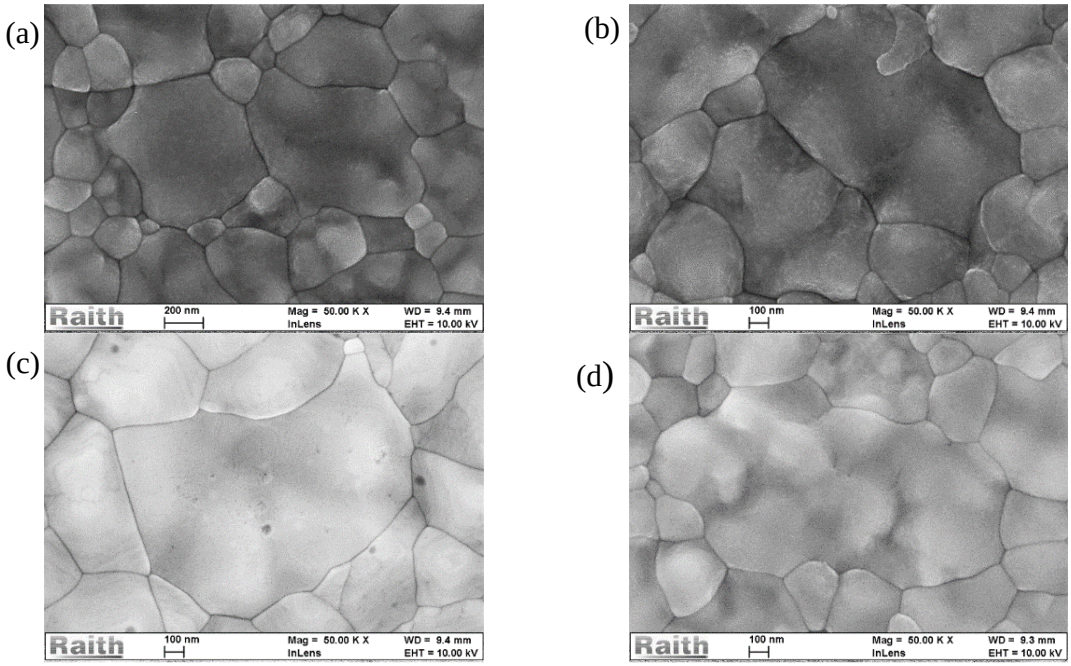

Fig. 3 SEM images after grain enhancement of CdSe thin films, (a) t: 0.5µm, GS ~1µm, (b) t: 1µm, GS ~1.3µm, (c) t: 2µm, GS ~1.5µm, (d) t: 3µm, GS ~19µm.

In Fig. 4, we show the cross-sectional SEM for one of the grain enhanced films, showing that the grain enhancement is through the entire film.

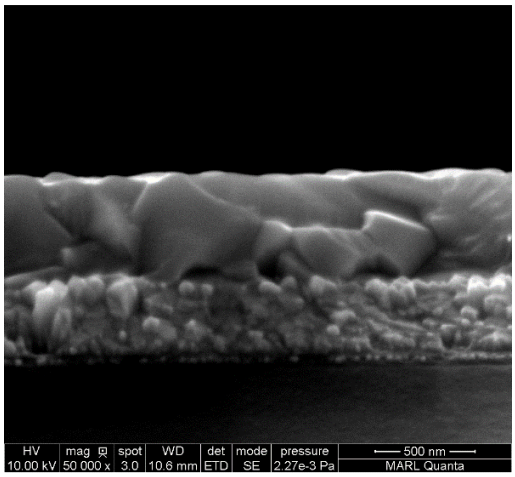

Fig. 4 Cross-section SEM of the grain enhanced CdSe thin film.

C. Electrical properties under grain enhancement

The electron mobility of CdSe films in the direction of growth was measured using the space charge limited current (SCLC) technique[11]. In this method, one uses a sample with ohmic contacts on both sides and measures current vs. voltage characteristic. When the injected charge density exceeds the thermal charge density, the current follows a J vs. V^2 relationship. The mobility can be calculated from the slope using Eq. (1), where J is the current density, V is the voltage, L is the sample length, $\epsilon = \epsilon_0 \epsilon_r$ where ϵ_0 is the absolute permittivity and ϵ_r is the relative permittivity of the material, and μ is the mobility of the carrier.

$$J = \frac{9}{8}\epsilon\mu \frac{V^2}{L^3} \quad (1)$$

Since CdSe is generally n-type, we used FTO/n^+-CdS/CdSe/PCBM/Al structure, where n^+ CdS and PCBM play roles as ohmic contacts on both sides for the n^+-n-n^+ structure as shown in Fig. 5.

Carrier concentration also can be measured using equation Eq. (2).

$$n = \epsilon \frac{1}{q} \frac{V_{SCLC}}{L^2} \quad (2)$$

Where n, q, and V_{SCLC} are carrier concentration, electron charge and voltage at space charge limited current region respectively.

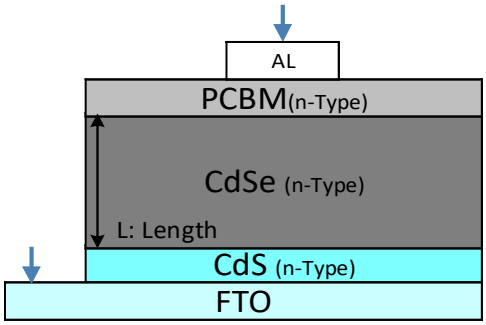

Fig. 5 Schematic diagram of n^+-n-n^+ structure to measure mobility of CdSe thin film using SCLC technique.

Fig. 6 shows current density vs. voltage and voltage square for as-deposited and grain-enhanced CdSe films for the films with thicknesses of 0.5µm, 1µm, 2µm, and 3µm. The figures show a distinct I vs. V^2 behavior at higher voltages. The slope of this line yields a value for mobility.

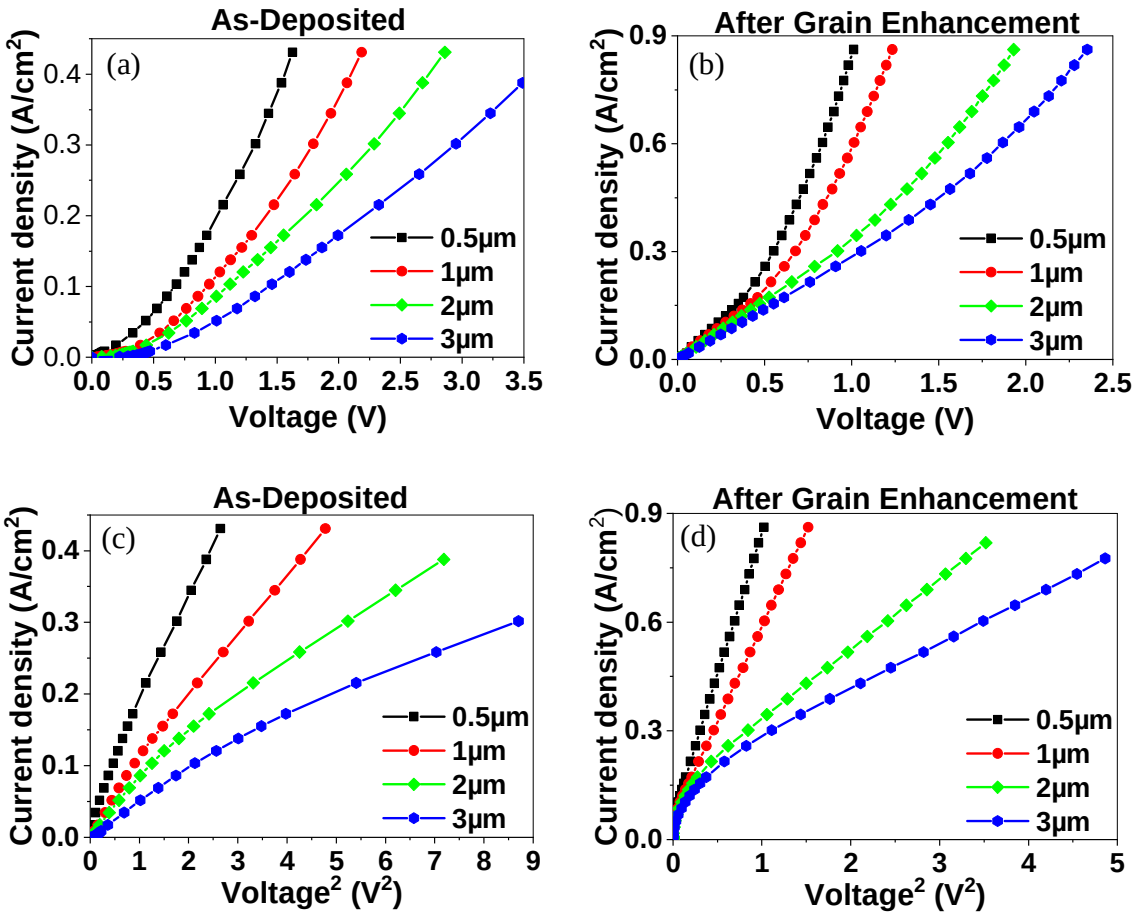

Fig. 6 I-V curves from SCLC experiment to measure mobility of CdSe films under four different thicknesses: 0.5µm, 1µm, 2µm, and 3µm. (a) J vs. V(as-deposited), (b) J vs. V (after grain enhancement), (c) J vs. V^2 (as-deposited), (d) J vs. V^2 (after grain enhancement).

Fig. 7(a) shows the mobility vs. thickness for as-deposited and after grain enhancement of CdSe thin films. Grain enhancement clearly leads to higher mobilities. Fig. 7(b) shows the mobility vs. grain size of CdSe thin films after grain enhancement. The highest mobility that we have achieved is about 3.5 $cm^2/V.S$ for large grain CdSe films in the range of 1.9-2µm.

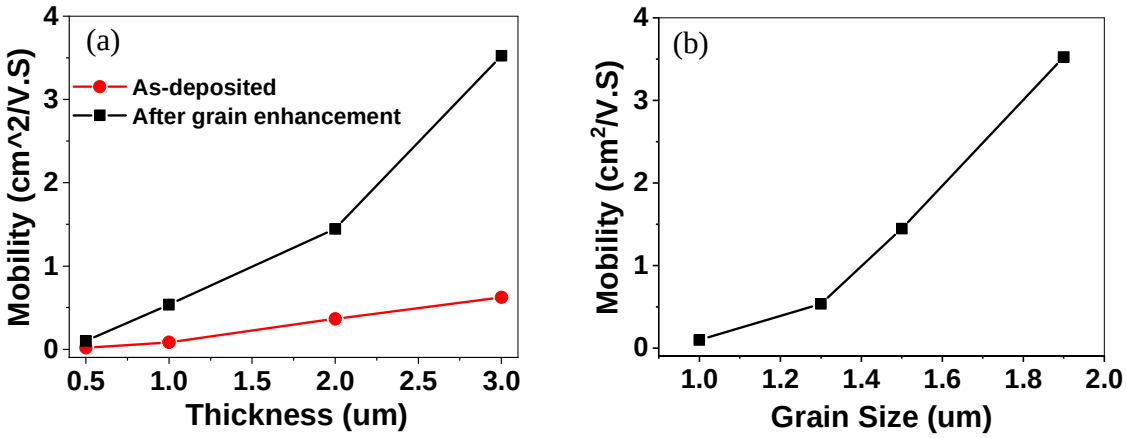

Fig. 7 Electron Mobility vs. film thickness (a) and Mobility vs. grain sizes (b) of CdSe thin films.

D. Influence of post grain growth selenization on photo and dark conductivity

Since the grain growth is done at relatively high temperatures, there is the potential loss of Se during such a procedure. To see if this is the case, one can measure dark and photo-conductivity of the films, and also study the tail state density, both after grain growth and after growth followed by selenization.

Photoconductivity was measured on as-deposited and after post-selenization of CdSe thin films. The results for photo-conductivity and light-to-dark conductivity ratio are shown in Fig. 8. It clearly shows that both photo-conductivity and light-to-dark conductivity increase as a function of selenization time. From the photo-conductivity, one can deduce the electron mobility-lifetime (μτ) product.

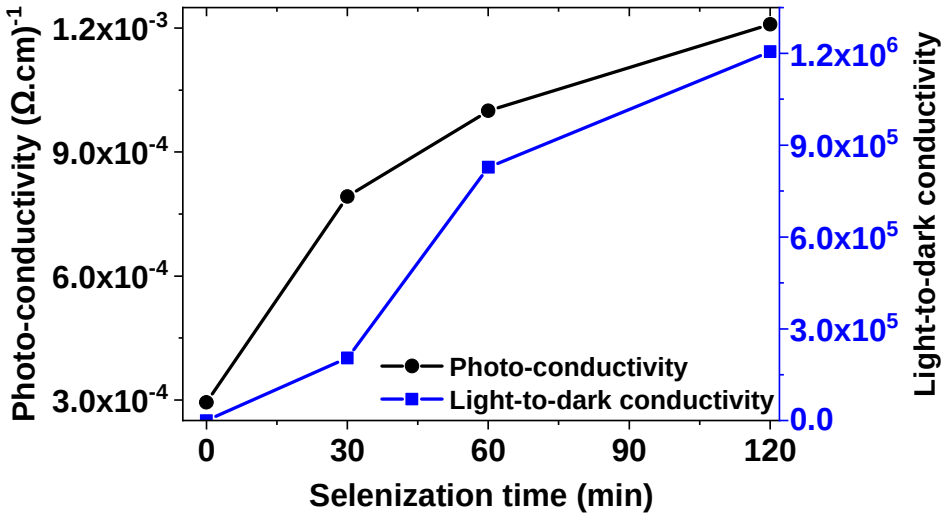

Fig. 8 Photo-conductivity and Light-to-dark conductivity of CdSe thin films for as-deposited and after post-selenization.

A large mobility-lifetime product indicates that the electron recombination center density has decreased. Mobility-lifetime product can be deduced from photo-conductivity by knowing the photon generation rate G/cm^3, given by:

$$G = \frac{N_{abs}}{t} \tag{3}$$

Where, N_{abs} is the number of absorbed photon flux and t the thickness of the film. The number of absorbed photos is given by:

$$N_{abs} = N_0\,(1 - R)(1 - \exp(-\alpha t)) \tag{4}$$

Where, No, R, α, and t are incident photon flux, reflection, absorption coefficient, and thickness respectively. Finally, photo-conductivity and Mobility-lifetime product can be expressed by

$$\Delta\sigma = \sigma_{Light} - \sigma_{Dark} \tag{5}$$

$$\mu\tau = \frac{\Delta\sigma}{qG} \tag{6}$$

Where, σ_{Light}, σ_{Dark}, and $\Delta\sigma$ are light conductivity, dark conductivity, and photo-conductivity respectively.

The mobility-lifetime product vs. post-selenization time curve is shown in Fig. 9. The figure shows that the (μτ) product increases by about 5 times after 120 minutes of selenization.

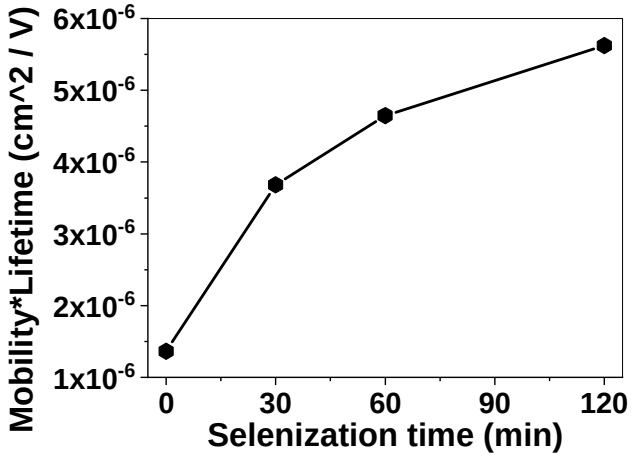

Fig. 9 Mobility-lifetime product vs. post-selenization time for CdSe thin film.

E. Measurement of tail state density

All polycrystalline materials have tail states near the conduction and valence bands because of the disorder in the crystalline network. For tail states near the valence band, which are filled with electrons since the material is n-type, an accurate way of measuring them is to use sub-bandgap photo-conductivity vs. photon energy[12]. The subgap photons excite electrons from the tail states into the conduction band, and assuming that the matrix elements coupling these states to the conduction band are independent of energy, a plot of subgap photo-conductivity vs. photon energy yields the density of tail states vs. energy. This method has been widely used to deduce tail state and mid-gap state densities in a-Si:H and perovskite[12,13].

In Fig. 10, we show the deduced density of tail states as a function of energy for three films, without grain enhancement, with grain enhancement, and with post-enhancement selenization.

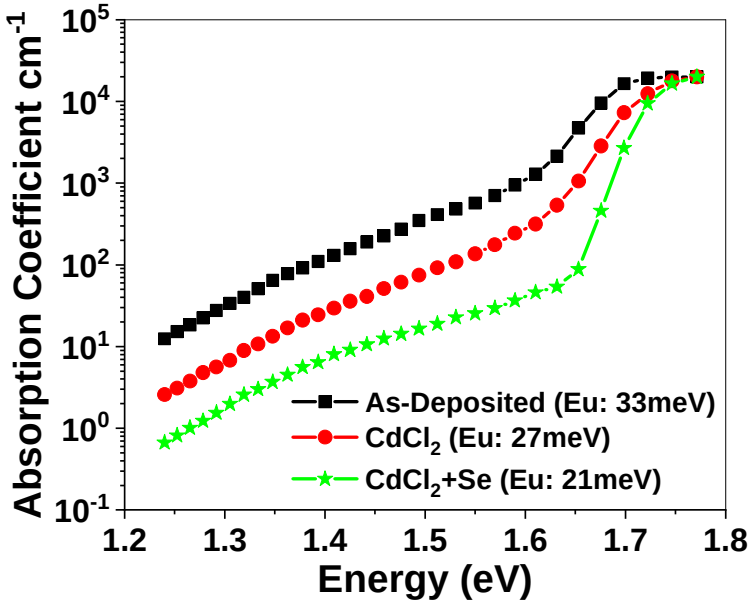

Fig. 10 Absorption coefficient vs. energy for three samples including As-Deposited, $CdCl_2$ Treated, and $CdCl_2$ Treated + Selenized samples.

The Urbach energy of tail states, E_u, which is deduced from the equation:

$$\alpha = \alpha_0 \exp(-\frac{E - E_c}{E_u}) \quad (7)$$

Where E_c is energy of conduction band. The Urbach energy is also reduced with selenization, and has a value of 21meV for the best film. This value is in the same range for other efficient photovoltaic materials such as perovksites[13].The figure also shows that at lower energies, there is flattening of the curve, indicating the presence of midgap states, and that selenization has also reduced the density of such states. This, of course is the reason why the electron ($\mu\tau$) product increased after selenization.

IV. Conclusions

CdSe thin films were prepared on glass and FTO/CdS substrates by thermal evaporation method at 400ºC under different thicknesses. The $CdCl_2$ heat treatment was carried out at 450ºC for different time inside a quartz tube in nitrogen atmosphere. It is seen that a high temperature heat treatment with $CdCl_2$ yields to significant grain enhancement. Selenization after grain-enhancement was shown to improve the photo-conductivity and the photo-to-dark conductivity ratio. Mobility-lifetime product for electrons was measured and was found to increase with selenization time, and be in the range of 5 x 10^{-6} cm^2/V. Tail state densities and Urbach energy of tail states near the valence band were measured and it was found that

selenization reduced the tail state densities and also reduced the midgap densities. The films had a low Urbach energy of 21meV after selenization.

Acknowledgements

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